

A BLOCK ORIENTED INTERFACE FOR CP/M* AND THE VADCG TERMINAL NODE CONTROLLER

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Abstract

This paper describes a system of hardware and software which provides for the transfer of blocks of data between a VADCG Terminal Node Controller (TNC) and a CP/M system with a serial interface. Both the software to run in the TNC and in the CP/M system is included. The system provides block transfers, data transparency, flow control and error checking and retransmission in both directions over the interface.

Introduction

The software to implement the Link level of protocol for the VADCG Terminal Node Controller was developed in 1978. It is now in general use both in the U.S. and Canada and has even been implemented on other Terminal Node Controller boards. It has proven to be satisfactory for the purposes intended but many people recognize the need to implement the next higher level of protocol - the Packet or Network level protocol.

There have been a large number of proposals as to the form this protocol should take and I have made my own proposals in a paper published in the last Amateur Radio Computer Networking Conference. In spite of a large supply of proposals there is a distinct shortage of implementations. Part of the reason for this has been because of the need for some kind of consensus in the Amateur Radio fraternity. Notwithstanding this important concern, there is another reason why we don't have our Network level protocol implemented - it is a lot of work to get it going.

'What are the problems in implementing the Network level protocol?', you may ask. Well, unlike the Link level protocol which only had to be implemented to run in a TNC, parts of the Network level protocol have to be implemented to run in each microcomputer connected to the network. Furthermore, the TIP programs in the TNCs will have to be rewritten and some changes in the LIP programs are needed as well. In addition, the Network level protocol is much more complex than the link level protocol. I think one of the main stumbling blocks is the need to implement the protocol on two separate systems before any testing can be done.

Despite the above difficulties, I have begun the process of implementing the protocol and have broken the job down into steps that can be implemented and tested and then proceed to the next step. To alleviate the problem of having to make two implementations for different systems, I am only making one implementation for my CP/M system which I will hopefully be able to transport to another local Packeteer's CP/M system for testing. In order to make this program as transportable as possible to other CP/M systems I am only using the 8080 instruction set.

The programs here are not really any part of a higher level protocol but the function they perform will be needed by any higher level protocol that is adopted. The microcomputer program called 'PACKET' is basically a set of drivers for the serial interface between the microcomputer and the TNC. The program implementing the higher level of protocol in the microcomputer is called the Transmission Control Program or TCP. The TCP will use these drivers to transfer blocks of data that it has prepared to the TNC and it will also receive blocks of data from the TNC using these drivers.

The TCP is called upon by the programs running in the microcomputer to send data and receive data

to and from various points in the network. In order to do this job, the TCP adds a header onto the outgoing blocks of data and because the bits and bytes in this header have a meaning based on their position in the block of data, there must be a mechanism to show where a block starts and ends in the serial data streams being passed across the interface between the computer and the TNC. This mechanism, was lacking in all the TIPs that I had access to. Also, since flexibility in the setting of these bits was needed and any kind of restriction on the data being sent across the interface was undesirable, there had to be a mechanism for data transparency. This mechanism, too, was missing in all the TIPs that I had access to. Also, since data was being sent both ways at high speed by microprocessors, there had to be a mechanism for flow control in both directions across the interface. Also, since my serial interface used long RS-232 cables in a noisy environment, I occasionally got bit errors in the data especially at the higher speeds so I needed to have error detection in this interface. In some environments, error detection may not be necessary but I decided to play it safe and include it. Finally, error detection is not of much use unless you can correct the errors so I have incorporated a retransmission mechanism.

To summarize - the interface provides the following:

1. Block recognition.
2. Data transparency.
3. Flow control (in both directions)
4. Error detection.
5. Error correction.

A block has the following format:

! SYN ! DLE ! STX ! DATA ! DLE ! ETX ! CRC ! PAD !
! 16H ! 10H ! 02H ! DATA ! 10H ! 03H ! CRC ! FFH !

The combination DLE-STX (ASCII Data Link Escape and Start of Text) indicates the start of a transparent block of data and the combination DLE-ETX indicates the end of the transparent block. To provide for data transparency a 'byte stuffing' technique is used - any time transparent data occurs that looks like a DLE, then an extra DLE is stuffed into the data stream. Therefore, the two byte combination DLE-DLE represents only a single data byte of 10H.

Flow control is accomplished using some hardware features of the TWC and the serial interface on the microcomputer. The RTS (Request to Send) and CTS (Clear to Send) lines are cross connected and controlled by the programs. When the output line is high it means 'You can send data to me now'. When the output line is low it means 'Don't send any data to me now.'

Error detection is accomplished using the two-byte CRC (Cyclic Redundancy Check) characters following the ETX character in the block. I am using the following polynomial to generate the CRC bytes:

$$x^{16} + x^{15} + x^2 + 1$$

This is the usual polynomial used for synchronous protocols such as IBM BISYNC but is not the one suggested by the CCITT. On transmit, the CRC calculation is done on all transmitted characters after the STX and up to and including the ETX character. The stuffed bytes are included in

the calculation and after the STX is processed, two bytes of zeroes are processed. On receive, the calculation is the same except that the two CRC bytes are used instead of the zero bytes and the result of the CRC calculation will then come out to zero if everything was received correctly.

The error correction mechanism employed also utilizes some of the hardware features of the TNC and the microcomputer. The DTR (Data Terminal Ready) and the DSR (DataSet Ready) lines are cross connected between the TNC and microcomputer. Whenever one side receives a block correctly, it reverses the state of its output line. If the other side does not detect the transition then, after a timeout, it retransmits the block.

Hardware Requirements

In order to use the program called 'TIPTTC' which runs in the VADCG TNC, you will need a VADCG TNC with the serial interface installed and an RS232 cable with wires going to the following pins installed (2,3,4,5,6,7 and 20).

In order to use the program called 'PACKET' which runs in a CP/M system, you will need to have a serial interface capable of handling 8-bit characters, direct software control of two lines of RS-232 levels, and the ability to read two input RS-232 lines with the software. Most CP/M systems have this capability. It is true that I could have written this software to only require the data lines (and I may yet do this) and the software would be slightly more transportable but more complicated and a little less efficient. The flow control and acknowledgment systems work very well because the software in the TNC is alerted by the interrupt system almost instantly when there is any change in level of the interface lines.

Software Requirements

The 'TIPTTC' program should interface with any of the common LIP programs being used with the VADCG board. I can only think of one thing to watch out for - the program uses variables in the CCA (Common Communications Area) from displacement 40H to 54H so you should check your LIP's usage of these areas and relocate them if your LIP uses part of the same area. Also, make sure your stack does not get extended down as low as displacement 54H in the CCA. This is a 'vanilla' TIP and in addition to the features described above, it only has provision for connect and disconnect. If you use this TIP you will have to do without those special functions you previously had. The other alternative is to add the functions to this program yourself. If you take this latter option I would very much like to hear from you as well as anyone else who uses these programs. I like to get 'feedback.'

The 'PACKET' program only needs a CP/M system with the aforementioned hardware features and some configuration modifications described in the next section.

Configuration Requirements

A. TIPTTC

A.1 At label 'BAUDRAT' the Baud rate may have to be changed. I am using 4800 Baud. In general it is best to have the rate as high as is reliable and convenient and should be **1200** or greater. However, lower Baud rates than **1200** would work as well.

A.2 At label 'ACKTO' there is a number which is related to the amount of time the TNC waits before retransmitting the block if no acknowledgment is received. This value has not been optimized from the first trial value. It is very non-critical and the value I chose for my system seems to work very well. It is probably quite a bit slower than required. You may experiment with different values.

A.3 At label 'RIMBUF' change the call sign to your own and if it is less than 6 characters, pad it on the right with blanks. Also, use upper case characters.

A.4 At label 'TERMNO' change your node number to whatever you want.

B. PACKET

B.1 In the section headed 'HARDWARE PORT EQUATES' you will have to change the port addresses to match the ports on your system.

B.2 In the sections headed 'CONTROL PORT BIT MEANINGS' and 'STATUS BIT MEANINGS' you will have to change the equates to match your system.

B.3 At label 'UARTINIT' change the code to initialize your serial interface UART to operate with 8 data bits and no parity bit. Also make the output lines going to pins 4 and 20 on the TNC are low. (The assumption here is that the jumper plug on the TNC is wired straight across)

B.4 At label 'SETRTS' change the code so that it makes pin 4 on the TNC end of the cable high.

B.5 At label 'CLEARRTS' change the code so that it makes pin 4 on the TNC end of the cable low.

B.6 At label 'FLIPDTR' make sure the code reverses the level on pin **20** of the TNC.

B.7 At label 'TESTTBE' test if data can be sent out to the UART and return non-zero status if it can.

B.8 At label 'TESTRDA' test if data is available from the UART and return non-zero status if it is.

B.9 At label 'TESTCTS' test the level of pin 5 coming from the TNC and return non-zero status if it is high.

B.10 At label 'TESTDSR' test the level of pin **6** coming from the TNC and compare it to the last tested level. If the value has changed, return non-zero status.

B.11 In routine 'KEYTEST' change the code to look for a character to be entered on your keyboard and if there is none, then go to 'OUTTEST'. It will probably have to be changed because my keyboard uses inverted logic.

Operation

Although the importance of the "PACKET" program lies in the features provided by the drivers in it, I have added 25 instructions which allow the program to provide an immediately useful function. It will allow the user to use the keyboard and screen display in the CP/M system as if it were a terminal connected directly to the TNC. Because of the power of the driver code, it is a relatively trivial matter to add this function. Similarly, a program to transfer a file from the system or to the system is very easy to implement using the drivers.

To use the program as a terminal simulator, simply type in a line of data on the keyboard, the line will be sent in a block to the TNC when the line feed key is pressed. While data is being entered after the first character, no blocks will be received from the TNC. While a block is being received from the TNC, the keyboard is not tested so a line that you enter will not be mixed with data coming from the TNC.

To connect, type the Call sign in upper case (which must be padded with blanks on the right if it is not 6 characters long) followed by control-A and then hit line feed to send it to the TNC. To disconnect, type any 6 characters (except for line feed) followed by control-B and then hit line feed. Sorry for this kludge but it is only temporary as I am planning to completely change the connect-disconnect procedures when I write the Transmission Control Program which is the next step in implementation of the Packet level protocols.

Summary

I hope these programs help those who are working on the implementation of the higher level protocols for an Amateur Radio digital communications network. It seemed to me that a program with these features would have to be one of the first steps in any kind of implementation but so far I have not heard of one. Perhaps someone out there has already written one and I have duplicated his effort. If so, then we are not doing enough advertising about what we have done. That is why I have taken this effort to disseminate the program.

The program listings here represent programs that have actually been running successfully so any problems encountered in transporting them to another system should be associated with the different environment and not with defects in the code. I can supply the programs on standard SS-SD CP/M format diskettes if necessary. Please enclose **\$3.00** with a blank diskette or \$8.00 without a diskette when making your request. You will find the listings for the two programs on the following pages.

* CP/M is a trade mark of Digital Research

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*****
** VADCG PACKET LEVEL TNC DRIVER FOR CP/M **
** BY DOUG LOCKHART, VE7APU JANUARY, 1983 **
***** LAST CHANGED JANUARY 31, 1983 *****
***** THIS PROGRAM CONTAINS THE DRIVERS TO EXCHANGE TRANS- ****
***** PARENT BLOCKS OF DATA BETWEEN A CP/M OPERATING ****
***** SYSTEM AND A VADCG TERMINAL NODE CONTROLLER USING A ****
***** MATCHING PROGRAM. IT USES THE REQUEST TO SEND (RTS) ****
***** AND CLEAR TO SEND (CTS) LINES FOR FLOW CONTROL AND ****
***** THE DATA SET READY (DSR) AND DATA TERMINAL READY ****
***** (DTR) LINES FOR ACKNOWLEDGEMENTS. ONLY DATA INFOR- ****
***** MATION IS PASSED ON THE DATA LINES. THE PROGRAM ****
***** USES 'BYTE STUFFING' TO ACHIEVE DATA TRANSPARENCY ****
***** AND USES A CRC-16 TO DETECT ERRORS. IF THE TRANS- ****
***** MITTED DATA IS NOT ACKNOWLEDGED BY A CHANGE IN LEVEL ****
***** THEN THE BLOCK IS SENT AGAIN. ****
***** MISCELLANEOUS EQUATES ****
0005 = LOS EQU 5
; ASCII EQUATES
000D = CR EQU ODH ; CARRIAGE RETURN
000A = LF EQU OAH ; LINE FEED
0010 = DLE EQU 10H ; DATA LINK ESCAPE
0002 = STX EQU 02H ; START OF TEXT
0003 = ETX EQU 03H ; END OF TEXT
0016 = SYN EQU 16H ; SYNCHRONIZING CHARACTER
00FF = PAD EQU OFFH ; PAD CHARACTER
***** HARDWARE PORT EQUATES ****
0001 = DATA EQU 01H ; UART DATA PORT
0000 = CONTROL EQU 00H ; UART CONTROL PORT
0000 = STATUS EQU 00H ; UART STATUS PORT
0002 = KEY BD EQU 02H ; KEYBOARD DATA PORT
; CONTROL PORT BIT MEANINGS
0001 = DTR EQU 01H ; NOT DATA TERMINAL READY
0002 = RTS EQU 02H ; NOT REQUEST TO SEND
0004 = BRS0 EQU 04H ; BAUD RATE SELECT
0008 = BRS1 EQU 08H ; BAUD RATE SELECT
0010 = WLS1 EQU 10H ; WORD LENGTH SELECT
0020 = WLS2 EQU 20H ; WORD LENGTH SELECT
0040 = SBS EQU 40H ; STOP BIT SELECT
0080 = PI EQU 80H ; PARITY INHIBIT
; STATUS BIT MEANING
0001 = RDA EQU 01H ; RECEIVE DATA AVAILABLE
0002 = KSTB EQU 02H ; NOT KEYBOARD STROBE
0004 = PE EQU 04H ; PARITY ERROR
0008 = FE EQU 08H ; FRAMING ERROR
0010 = OE EQU 10H ; OVERRUN ERROR
0020 = DSR EQU 20H ; NOT DATA SET READY
0040 = CTS EQU 40H ; NOT CLEAR TO SEND
0080 = TBE EQU 80H ; TRANSMIT BUFFER EMPTY
***** ORG 100H ****
0100 31C903 ORG 100H
0103 CD4301 LXX SP,STACK ; INITIALIZE STACK
0106 CD3501 CALL UARTRINIT ; INITIALIZE UART
0109 CA2301 OUTTEST:CALL WRITESTAT ; ANY DATA IN TBUP?
010C DB00 JZ LINETEST ; NO, TRY TO RECEIVE SOME
KEYTEST:IN STATUS ; ANY KEYBOARD DATA?
010E E602 AN1 KSTB
0110 C20601 JNZ OUTTEST ; NO, TEST FOR LINE DATA
0113 DB02 IN KEYBD ; GET DATA
0115 CD3A01 CALL DISPLAY ; DISPLAY IT
0118 CD3A05 CALL WRITE ; PUT IT INTO BUFFER
011B FEOA CPI LF ; WAS IT A LINE FEED?
011D CC1005 cz TCLOSE ; YES, SEND DATA IN BUFFER
0120 C30601
0123 CD3505
0126 CC3A04
0129 CA0C01
012C CD1805
012F CD3A01
0132 C32301
0135 3A9B02
0138 B7
0139 C9
013A F5
013B 5F
013C 0E02
013E CD0500
0141 F1
0142 C9
0143 3EB7
0145 D300
0147 329801
014A DB01
014C DB00
014E E620
0150 329701
0153 C9
0154 3A9801
0157 E6FD
0159 D300
015B 329801
015E C9
015F 3A9801
0162 F602
0164 8300
0166 329801
0169 C9
016A 3A9801
016D EE01
016F D300
0171 329801
0174 C9
0175 DB00
0177 E680
0179 C9
017A DB00
017C E601
017E C9
017F DB00
0181 E640
0183 FE40
0185 C9
; LINETEST: CALL READSTAT ; DATA IN RECEIVE BUFFER?
; CZ BLOCKRX ; NO, TRY TO RECEIVE SOME
; JZ KEYTEST ; NO, TEST KEYBOARD ENTRY
; CALL READ ; GET DATA BYTE FROM RBUF
; CALL DISPLAY ; AND DISPLAY IT
; JMP LINETEST
; WRITESTAT: LDA TBUFNUM ; GET COUNT
; ORA A ; AND TEST IT
; RET
; DISPLAY: PUSH PSW
; MOV E,A
; MVI C,2
; CALL BIOS ; DISPLAY DATA IN (E)
; POP PSW
; RET
; RETURN TO CALLER
; BASIC UART DRIVER ROUTINES
; INITIALIZATION OF UART
; UARTRINIT: MVI A,PI+WLS1+WLS2+BRS0+DTR+RTS ; 8 DATA,
; OUT CONTROL ; NO PARITY, DIR AND RTS OFF
; STA CTRL ; SAVE CONTROL INFO
; IN DATA ; CLEAR ANY RESIDUAL DATA
; IN STATUS ; SAVE INITIAL DSR STATUS
; ANI DSR
; STA DSRSTAT
; RET
; RETURN TO CALLER
; ENABLE RTS (MEANS DATA CAN BE RECEIVED)
; SETRTS: LDA CTRL ; GET CONTROL INFORMATION
; ORI AN1 OFFH-RTS
; OUT CONTROL
; STA CTRL
; RET
; DISABLE RTS (MEANS DO NOT SEND ME ANY DATA )
; CLEARRTS: LDA CTRL ; GET CONTROL INFORMATION
; ORI RTS
; OUT CONTROL
; STA CTRL
; RET
; REVERSE VALUE OF DTR (TO ACKNOWLEDGE BLOCK )
; FLIPDTR:LDA CTRL ; GET CONTROL INFORMATION
; XRI DTR ; FLIP DTR
; OUT CONTROL
; STA CTRL ; SAVE UART CONTROL INFORMATION
; RET
; RETURN TO CALLER
; TEST VALUE OF TBE (TRANSMIT BUFFER EMPTY)
; TESTTBE:IN STATUS
; ANI TBE
; RET
; TEST IF RECIEVE DATA IS AVAILABLE
; TESTRDA:IN STATUS
; ANI RDA
; RET
; TEST VALUE OF CLEAR TO SEND
; TESTCTS:IN STATUS
; AN1 CTS
; CPI CTS
; NOTE SENSE INVERTED
; RET

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; TEST IF VALUE OF DATA SET READY HAS CHANGED
 ; NON-ZERO FLAG IF DSR HAS CHANGED, ZERO IF NOT
0186 E5
0187 C5
0188 219701
018B 46
018C DB00
018E E620
0190 77
0191 B8
0192 C1
0193 E1
0194 C9
0195 0000
0197 00
0198 00
00FA = MAXNUM EQU 250
0199 9C01
RPOINT: DW RBUF
019B 00
RBUFN:DB 0
019C RBUF: DS 253
0299 9C02
TPOINT: DW TBUF
029B 00
TBUFN:DB 0
029C TBUF: DS 253
0399 STACK EQU \$
03C9 =

 ; SEND BYTE OF DATA OUT TO SERIAL PORT
 ; DATA PASSED IN ACCUMULATOR
 ;
 SENDDATA:
03C9 CD5205
03CC E5
03CD C5
03CE 4F
03CF 210100
03D2 2B
03D3 7C
03D4 B5
03D5 C2D203
03D8 CD7501
03DB CAD803
03DE CD7F01
03E1 CADE03
03E4 79
03E5 D301
03E7 C1
03E8 E1
03E9 C9
 ;
 ; SEND DATA IN TBUF TO THE UART TRANSPARENTLY
 ;
 SENDTBUF:
03EA E5
03EB C5
03EC 219B02
03EF 4E
 SENDTBUF1:
03F0 23
03F1 7E
03F2 CDC903
03F5 FE10
03F7 CCC903
03FA 0D
03FB C2F003
03FE C1
03FF E1
0400 C9
 SEND FORMATTED BLOCK TO UART
 BLOCKTX:
0401 3E16
 MVI A,SYN

0403 CDCC03
0406 3E10
0408 CDCC03
040B 3E02
040D CDCC03
0410 210000
0413 229501
0416 CDEA03
0419 3E10
041B CDC903
041E 3E03
0420 CDC903
0423 CDDE04
0426 CDF204
0429 CDD004
042C CA0104
042F AF
0430 329B02
0433 219C02
0436 229902
0439 C9

 ; READ A FORMATTED TRANSPARENT BLOCK OF DATA
 BLOCKRX: CALL SETRTS ; ALLOW OTHER END TO SEND
 BLOCKRX1:
 CALL RECEIVE ; READ A BYTE FROM LINE
0440 C8 RZ ; RETURN WITH ZERO STATUS IF TIMED OUT
0441 FE10 CPI ; IS IT DLE?
0443 C23D04 JNZ BLOCKRX1 ; NO, KEEP TRYING
0446 CDAE04 CALL RECEIVE ; GOT DLE, TRY FOR STX
0449 C8 RZ ; RETURN WITH ZERO STATUS IF TIMED OUT
044A FE02 CPI ; IS IT STX?
044C C23D04 JNZ BLOCKRX1 ; NO, TRY FOR DLE AGAIN
 BLOCKRX2:
 LX1 H,RBUF ; POINT TO START OF RBUF
044F 219C01 SHLD RPOINT ; RECEIVE DATA INTO RBUF
0452 229901 CALL RCVRBUF ; UNTIL A CONTROL SEQUENCE IS RECEIVED
0455 CD8004 CALL RECEIVE ; RETURN ZERO STATUS IF LINE TIMES OUT
 RZ ETX ; WAS IT FTX?
0458 C8 CPI ; UNEXPECTED SEQUENCE
0459 FE03 JNZ BLOCKRX1 ; RECEIVE FIRST CRC CHAR
045B C23D04 CALL RECEIVE ; RETURN HERE IF TIME OUT
045E CDAE04 RZ CALL RECEIVE ; RECEIVE SECOND CRC CHAR
0461 C8 RZ CALL CLEARRTS ; RETURN HERE IF TIME OUT
0462 CDAE04 LHLD CRC ; STOP OTHER END
0465 C8 MOV A,H ; CHECK IF CRC WAS OK
0466 CD5F01 ORA L ;
0469 2A9501 JNZ BLOCKRX3 ; NO GOOD
0470 219B01 LX1 H,RBUFNUM ; SAVE DATA COUNT
0471 219B01 MOV M,C ;
0472 71 CALL FLIPDTR ; GOOD, REVERSE DTR LINE
0473 CD6A01 MVI A,-1 ; TO ACKNOWLEDGE BLOCK
 MVI A ; RETURN NON-ZERO STATUS
 ORA A ; BLOCK RECEIVED OK
 RET ; RETURN TO CALLER
 BLOCKRX3:
 MVI A,0 ; RETURN WITH ZERO STATUS
 ORA A ; NO BLOCK RECEIVED
 RET ;
 ; RECEIVE DATA PORTION OF BLOCK, RETTJRNS WHEN A
 ; CONTROL SEQUENCE FOUND IN THE TRANSPARENT TEXT
 RCVRBUF: LXI H,0 ; INITIALIZE CRC TO 0
 SHLD CRC ;
 LXI H,RBUF ; POINT TO START OF RBUF
 MVI C,0 ; BYTE COUNT = 0
 RCVREUTY: CALL RECEIVE ; GET A BYTE FROM LINE
 Rz ; RETURN HERE WITH ZERO STATUS IF TIMEOUT

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048F FE10          CPI    DLE      ; WAS IT DLE?
0491 CA9A04        JZ     RCVRBUF3   ; YES, LOOK AT NEXT BYTE
0494 77           MOV    M,A      ; PUT INTO BUFFER
0495 23           INX    H       ; INCREMENT REBUF POINTER
0496 OC           INR    C       ; INCREMENT COUNT
0497 C38B04        JMP    RCVRBUF1  ; LOOP FOR NEXT BYTE
049A CDAE04        RCVRBUF2: CALL   RECEIVE
049D C8           RZ      ; ZERO STATUS RETURN IF LINE TIMES OUT
049E FE10        CPI    DLE      ; IS IT A TRANSPARENT DLE?
04A0 CA9404        JZ     RCVRBUF2  ; YES, GO PUT INTO BUFFER
04A3 C9           RET      ; RETURN WITH CONTROL BYTE IN ACCUMULATOR
04A4 E5           TRY TO READ PROM LINE WITH LONG TIMEOUT
04A5 CD5401        RECEIVL: PUSH  H
04A8 21A00F        CALL   SETRTS   ; ALLOW OTHER END TO SEND
04AB C3B504        LXI    H,4000   ; LONG TIMEOUT VALUE
04AE E5           TRY TO READ FROM LINE, IF LINE TIMES OUT,
04AF CD5401        RECEIVE: PUSH  H
04B2 210007        CALL   SETRTS   ; ALLOW OTHER END TO SEND
04B5 CD7A01        RECEIV1: CALL  TESTRDA ; ADJUST FOR ABOUT 2 CHAR TIMES
0488 CAC204        JZ     RECEIV2   ; ANY RECEIVED DATA?
04BB DBO?          IN     DATA      ; GET DATA BYTE
04BD CD5205        CALL   CALCCRC  ; INCLUDE IT IN CRC
04C0 E1           POP    H
04C1 C9           RET      ; GOOD RETURN WITH NON ZERO STATUS
04C2 2B           RECEIV2: DCX   H
04C3 7C           MOV    A,H      ; DECREMENT TIMER
04C4 B5           ORA    L       ; IS TIME OVER
04C5 C2B504        JNZ    RECEIV1   ; NO, KEEP TRYING
04C8 CD5F01        CALL   CLEARRTS; OOPS, TIMED OUT,
04CB 3E00          MVI    A,0      ; DROP RTS SO OTHER SIDE WILL STOP
04CD B7           ORA    A
04CE E1           POP    H
04CF C9           RET      ; RETURN WITH ZERO STATUS
04D0 011027        WAITDSR: WAITDSR? LXI    B, 10000 ; DELAY - ALTER AS REQ'D
04D3 CD8601        WAITDSR?: CALL   TESTDSR  ; CHECK FOR DSR CHANGE
04D6 CO           RNZ    ; RETURN IF IT HAS
04D7 0B           DCX   B
04D8 78           MOV    A,B      ; IS TIME OVER?
04D9 B1           ORA    C
04DA C2D304        JNZ    WAITDSR1 ; NO CONTINUE TESTING
04DD C9           RET      ; UNSUCCESSFUL RETURN
04DE AF           SENDCRC: XRA   A
04DF CD5205        SENDCRC: CALL   CALCCRC ; FINISH CRC CALCULATION
04E2 CD5205        CALL   CALCCRC
04E5 3A9601        LDA    CRC+1   ; SEND FIRST CRC CHAR
04E8 CDCC03        CALL   SEND     ; SEND SECOND CRC CHAR
04EB 3A9501        LDA    CRC     ; SEND
04EE CDCC03        CALL   SEND     ; SEND
04F1 C9           REX
04F2 3A9B01        CHECKRX: LDA   RBUFNFM ; IS THERE ANY DATA LEFT
04F5 B7           CPI    DLE      ; IN RECEIVE BUFFER?
04F6 C0           RNZ   CALL    ; YES, CAN'T RECEIVE
04F7 CD5401        SETRTS
04FA CDA404        CHECKRX1: CALL   RECEIVL ; READ WITH LONG TIMEOUT
04FD C8           RZ      ; TIMED OUT, RETURN
04FE FE10        CPI    DLE      ; IS IT A DLE?
0500 C2FA04        JNZ    CHECKRX1 ; NO, KEEP LOOKING
0503 CDA404        CALL   RECEIVL ; NOW LOOK FOR A STX
0506 C8           RZ      ; TIMED OUT SO RETURN
0507 FE02        CPI    STX      ; IS IT START OF TEXT?
0509 C2FA04        JNZ    CHECKRX1 ; NO, KEEP LOOKING
050C CD4F04        CALL   BLOCKRX2 ; NOW GO READ TRANSP.TEXT
050F C9           RET      ; ZERO STATUS IF TIMEOUT
0510 3A9B02        TCLOSE: LDA   TBUFNFM ; SEND A BLOCK OF TRANSMIT DATA TO THE LINE?
0513 B7           ORA    A       ; THERE IS ANY DATA IN THE BUFFER
0514 C40104        CNZ    BLOCKTX ; GET COUNT IN BUFFER
0517 C9           RET      ; TEST FOR DATA
0518 ES           READ: PUSH  H
0519 219B01        READ1: LXI   RBUFNFM ; SEND BLOCK IF ANY DATA
051C 7E           MOV    A,M      ; RETURN TO CALLER
051D B7           ORA    A
051E C22A05        JNZ    READ2   ; IS THERE MY LEFT?
0521 CD1005        CALL   TCLOSE  ; YES
0524 CD3A04        CALL   BLOCKRX ; SEND ANY DATA IN TBUF
0527 C31905        JMP    READ1  ; RECEIVE ANOTHER BLOCK
052A 35           DCR    M       ; TRY TO DO READ AGAIN
052B 2A9901        LHLD   RPOINT ; DECREMENT COUNT
052E 7E           MOV    A,M      ; GET READ POINTER
052F 23           INX    H       ; GET DATA BYTE
0530 229901        SHLD   RPOINT ; INCREMENT POINTER
0533 E1           POP    H       ; AND SAVE AGAIN
0534 C9           RET      ; RESTORE HL
0535 3A9B01        READSTAT: LDA   RBUFNFM ; RETURN TO CALLER WITH DATA IN A
0538 B7           ORA    A
0539 C9           RET      ; NON-ZERO STATUS IF DATA PRESENT
053A F5           WRITE: PUSH  PSW   ; SAVE DATA
053B E5           PUSH  H       ; SAVE HL
053C 2A9902        LHLD   TPOINT ; GET POINTER INTO TBUF
053F 77           MOV    M,A      ; PUT DATA INTO BUFFER
0540 23           INX    H       ; INCREMENT POINTER
0541 229902        SHLD   TPOINT ; POINT TO COUNT IN TBUF
0544 219B02        LXI   H,TBUFNFM ; INCREMENT COUNT
0547 7E           MOV    A,M      ; IS BUFFER FULL?
0548 3C           INR    A       ; YES, SEND BLOCK NOW
0549 77           MOV    M,A      ; RESTORE HL
054A FEFA        CPI    MAXNUM ; RESTORE DATA
054C cc0104        CALL   BLOCKTX
054F E?           POP    H
0550 F1           POP    PSW   ; RESTORE DATA
0551 C9           RET
0552 E5           ; CRC CALCULATION ROUTINE
0553 C5           ; USES BYTE PASSED IN ACCUMULATOR TO INCLUDE IN CRC
0554 F5           ; RESTORES ALL REGISTERS AND STATUS
0555 0608        CALCCRC: PUSH  H
0557 4F           PUSH  PSW   ; RESTORE DATA
0558 2A9501        MVI    B,8    ; RESTORE DATA
055B =             MOV    C,A    ; RESTORE DATA
055B 79           LHLD   CRC   ; RESTORE DATA
04F2 3A9B01        CALCCRC1: EQU   $ ; RESTORE DATA
04F2 3A9B01        MOV    A,C

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055C 07          RLC
055D 4F          MOV C,A
055E 7D          MOV A,L
055F 17          RAL
0560 6F          MOV L,A
0561 7C        MOV A,H
0562 17          RAL
0563 67          MOV H,A
0564 D26F05      JNC CALCCRC2
0567 7C          MOV A,H
0568 EE80        XRI 80H
056A 67          MOV H,A
056B 7D          MOV A,L
056C EE05        XRI 05H
056E 6F          MOV L,A
CALCCRC2:       DCR B
056F 05          JNZ CALCCRC1
0570 C25B05      SHLD CRC
0573 229501      POP PSW
0576 F1          POP B
0577 C1          POP H
0578 E1          POP
0579 C9          RET
057A             END

; **** VADCG TERMINAL NODE COMMUNICATIONS PROGRAM ***
; ** BY DOUG LOCKHART, VE7APU JANUARY, 1983 ***
; **** LAST CHANGED: JANUARY 31, 1983 ***
; **** TERMINAL INTERFACE PROGRAM FOR INTERFACING TO A CP/M
; SYSTEM. THIS PROGRAM IS WRITTEN TO RUN IN THE VADCG
; TERMINAL NODE CONTROLLER. IT INTERFACES WITH A LINK
; INTERFACE PROGRAM (LIP) RUNNING AT ADDRESS 0 IN MEMORY.
; THIS VERSION IS WRITTEN TO USE THE 8250 PROGRAMMABLE
; UART TO COMMUNICATE WITH A COMPUTER.
; THE BASIC FEATURES OF THIS TIP ARE:
; TRANSFER OF DATA IN BLOCKS
; RTS FLOW CONTROL FROM DIGITAL EQUIPMENT TO TIP
; AND CTS FLOW CONTROL FROM TIP TO DIGITAL EQUIPMENT
; ACKNOWLEDGEMENTS TO BLOCKS RECEIVED BY A CHANGE IN DTR
; ACKNOWLEDGEMENTS TO BLOCKS SENT BY A CHANGE IN DSR
; CRC-16 CHECKING OF ALL DATA BLOCKS
; ERROR RECOVERY BY RETRANSMISSION IF NO ACKNOWLEDGMENT
; USES BYTE STUFFING TECHNIQUE FOR DATA TRANSPARENCY

INCTB MACRO ?D
IF NOT NUL ?D
MVI A,?D
ENDIF
RST 2
ENDM

INCLB MACRO ?D
IF NOT NUL ?D
MVI A,?D
ENDIF
RST 3
ENDM

COMPARE MACRO
RST
ENDM
5

SIM MACRO
DB 30H ; SET INTERRUPT MASK
ENDM

RIM MACRO
DB 20H ; READ INTERRUPT MASK
ENDM

1000 = ; RAM CONSTANT - CHANGE FOR DIFFERENT RAM LOCATION
LORAM EQU 1000H ; START OF RAM STORAGE

; NON-ZERO STATUS MEANS LINE BUFFER ADDRESS IS IN HL REG.
; ZERO STATUS MEANS NO BUFFER IS READY
NEXTIN MACRO
RST 4
ENDM

; 8255 PARALLEL I/O EQUATES
0008 = PORTA EQU 8 ; PORT A INPUT AND OUTPUT
0009 = PORTB EQU 9 ; PORT B INPUT AND OUTPUT
000A = PORTC EQU 0AH ; PORT C INPUT AND OUTPUT
000B = CONTROL EQU 0BH ; CONTROL PORT OUTPUT ONLY

0004 = ; BAUD RATE EQUATES
BAUD384 EQU 4 ; DIVISOR FOR 38,400 BAUD
0008 = BAUD192 EQU 8 ; DIVISOR FOR 19,200 BAUD
0010 = BAUD96 EQU 16 ; DIVISOR FOR 9600 BAUD

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0020	=	BAUD48	EQU	32	;	DIVISOR	FOR	4800	BAUD
0040	=	BAUD24	EQU	64	;	DIVISOR	FOR	2400	BAUD
0080	=	BAUD12	EQU	128	;	DIVISOR	FOR	1200	BAUD
0100	=	BAUD600	EQU	256	;	DIVISOR	FOR	600	BAUD
0200	=	BAUD300	EQU	512	;	DIVISOR	FOR	300	BAUD
0400	=	BAUD150	EQU	1024	;	DIVISOR	FOR	150	BAUD
0476	=	BAUD134	EQU	1142	;	DIVISOR	FOR	134.5	BAUD
0573	=	BAUD110	EQU	1395	;	DIVISOR	FOR	110	BAUD
0800	=	BAUD75	EQU	2048	;	DIVISOR	FOR	75	BAUD
0C00	=	BAUD50	EQU	3072	;	DIVISOR	FOR	50	BAUD

; 8250 SERIAL I/O EQUATES

; REGISTER EQUATES			
0000 =	RBR	EQU	0
0000 =	THR	EQU	0
0001 =	IER	EQU	1
0002 =	IIR	EQU	2
0003 =	LCR	EQU	3
0004 =	MCR	EQU	4
0005 =	LSR	EQU	5
0006 =	MSR	EQU	6
0000 =	DLL	EQU	0
0001 =	DLM	EQU	1
			; RECEIVE BUFFER REGISTER (R)
			; TRANSMIT HOLDING REGISTER (W)
			; INTERRUPT ENABLE REGISTER (W)
			; INTERRUPT IDENT. REGISTER (R)
			LINE CONTROL REGISTER (R/W)
			MODEM CONTROL REGISTER (R/W)
			LINE STATUS REGISTER (R/W)
			MODEM STATUS REGISTER (R/W)
			; DRIVER LATCH (LSB) (W)
			DRIVER LATCH (MSB) (W)

~~; INTERRUPT ENABLE EQUATE~~

0001 = ERBFI EOU 1 ; ENABLE RECEIVED DATA INTERRUPT
0002 = ETBEI EOU 2 ; ENABLE TRANSMITTER
0004 = ELSI EOU 4 ; RECEIVER LINE STATUS INTERRUPT
0008 = EDSSI EOU 8 ; ENABLE MODEM STATUS INTERRUPT

; INTERRUPT IDENTIFICATION EQUATES

0001 = IPEND EQU 1 ; '0' IF INTERRUPT PENDING
0002 = IID0 EQU 2 ; INTERRUPT IDENTIFICATION BIT 0
0004 = IID1 EQU 4 ; INTERRUPT IDENTIFICATION BIT 1

; LINE CONTROL EQUATES

0001	=	WLS0	EQU	1	WORD LENGTH SELECT BIT 0
0002	=	WLS1	EQU	2	WORD LENGTH SELECT BIT 1
0004	=	STB	EQU	4	STOP BIT SELECT
0008	=	PEN	EQU	8	PARITY ENABLE
0010	=	EPS	EQU	10H	EVEN PARITY SELECT
0020	=	SPTY	EQU	20H	STICK PARITY
0040	=	SBRK	EQU	40H	SET BREAK
0080	=	DLAB	EQU	80H	DRIVER LATCH ACCESS BIT

; MODEM CONTROL EQUATES

```

0001 = DTR EQU 1 ; DATA TERMINAL READY
0002 = RTS EQU 2 ; REQUEST TO SEND
0004 = OUT1 EQU 4 ; OUT1 LINE ON 8250
0008 = OUT2 EQU 8 ; OUT2 LINE ON 8250
0010 = LOOP EQU 10H ; MODEM LOOP CONTROL BIT

```

; LINE STATUS EQUATES

0001	=	DR	EQU	1	DATA READY
0002	=	OE	EQU	2	OVERRUN ERROR
0004	=	PE	EQU	4	PARITY ERROR
0008	=	FE	EQU	8	FRAMING ERROR
0010	=	BI	EQU	10H	BREAK INTERRUPT
0020	=	THRE	EQU	20H	TRANSMITTER HOLDING REG EMPTY
0040	=	TSRE	EQU	40H	TRANSMITTER SHIFT REG EMPTY

; MODEM STATUS EQUATES

```

0001 = DCTS EQU 1 ; DELTA CLEAR TO SEND
0002 = DDSR EQU 2 ; DELTA DATA SET READY
0004 = TERI EQU 4 ;.TRAILING EDGE RING INDICATOR
0008 = DRLSD EQU 8 ; DELTA RX LINE SIGNAL DETECT
0010 = CTS EQU 10H ; CLEAR TO SEND
0020 = DSR EQU 20H ; DATA SET READY
0040 = RI EQU 40H ; RING INDICATE

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0080 =      RLSD   EQU    80H    ; RECEIVE LINE SIGNAL DETECT
0017 =      RIMD   EQU    17H    ; REQUEST INITIALIZATION MODE
0008 =      MSE    EQU    08H    ; MASK SET ENABLE BIT

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COMMON COMMUNICATIONS AREA

CIRCULAR TERMINAL BUFFER VARIABLES

1000 =	CCA	EQU	LORAM	; COMMON COMMUNICATIONS AREA ADR.
1004 =	CTBIE	EQU	CCA+4	; CURRENT TERMINAL BUF INP. ENTRY
1006 =	OTBE	EQU	CCA+6	; OLDEST TERMINAL BUFFER ENTRY
1008 =	TBIP	EQU	CCA+8	; TERMINAL BUFFER INPUT POINTER
100A =	TBOP	EQU	CCA+0AH	; TERMINAL BUFFER OUTPUT POINTER
100C =	LTBOE	EQU	CCA+0CH	; LAST TERMINAL BUF OUTPUT ENTRY
100E =	CTBOE	EQU	CCA+0EH	; CURRENT TERMINAL BUF OUT ENTRY

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; CIRCULAR LINE BUFFER VARIABLES

LBPE    EQU    CCA+12H ; LINE BUFFER PROCESSING ENTRY
CLBE    EQU    CCA+14H ; CURRENT LINE BUFFER ENTRY ADDR.
OLBE    EQU    CCA+16H ; OLDEST LINE BUFFER ENTRY
LBIP    EQU    CCA+18H ; LINE BUFFER INPUT POINTER
LBOP    EQU    CCA+1AH ; LINE BUFFER OUTPUT POINTER
```

MISCELLANEOUS

1000 = STAT1 EQU CCA ; MAINLINE STATUS BYTE
; THE FOLLOWING VARIABLES ARE FOR EXCLUSIVE USE BY TIP

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101C = BUFCOUNT EQU CCA+1CH ; CURRENT INPUT BUFFER COUNT
101D = OUTCOUNT EQU CCA+1DH ; CURRENT OUTPUT BYTES REMAINING
1040 = WAIT EQU CCA+40H ; CHARACTER DELAY VALUE
1042 = MSRSAVE EQU CCA+42H ; LATEST MODEM STATUS REGISTER
1043 = INTFLAG EQU CCA+43H ; INTERRUPT ROUTINE FLAGS
0001 = RXBUSY EQU 01H ; RECEIVE INTRPT ROUTINE ACTIVE
0002 = TXBUSY EQU 02H ; TRANSMIT INTRPT ROUTINE ACTIVE
1044 = CRC EQU CCA+44H ; CRC CALCULATION AREA
1046 = RCRC2 EOU CCA+46H ; SECOND RECEIVED CRC BYTE
1047 = RCRC1 EOU CCA+47H ; FIRST RECEIVED CRC BYTE
1048 = TCR2 EQU CCA+48H ; SECOND TRANSMIT CRC BYTE
1049 = TCR1 EOU CCA+49H ; FIRST TRANSMIT CRC BYTE
104A = RNEXT EQU CCA+4AH ; CURRENT RECEIVE ROUTINE ADDRESS
104C = TNEXT EOU CCA+4CH ; TRANSMIT ROUTINE ADDRESS
104E = RDISP EOU CCA+4EH ; RECEIVE INTERRUPT ROUTINE ADDR.
1050 = TDISP EOU CCA+50H ; TRANSMIT INTERRUPT ROUTINE ADDR.
1052 = DFLAG EQU CCA+52H ; DISPATCH FLAG
0001 = CRCTY EOU 01H ; CRC ROUTINE IN USE BY TX DISP

```

; ASCII EQUATES			
000D =	CR	EQU	ODH
000A =	LF	EQU	0AH
001B =	ESC	EQU	1BH
0002 =	STX	EQU	02H
0003 =	ETX	EQU	03H
0010 =	DLE	EQU	10H
0016 =	SYN	EQU	16H
00FF =	PAD	EQU	0FFH
			; CARRIAGE RETURN
			; LINE FEED
			; ESCAPE CHARACTER
			; START OF TEXT
			; END OF TEXT
			; DATA LINK ESCAPE
			; SYNCHRONIZATION CHARACTER
			; TRAILING PAD CHARACTER
0OFF =	TRUE	EQU	0FFH
0000 =	FALSE	EQU	0
			; FOR IF CONDITION TESTS
			; FOR IF CONDITION TESTS

; *****
; ** CONFIGURATION EQUATES
; ** VALUES CHANGE FOR EVERY CONFIGURATION
; *****

0003 = FORMAT EQU WLS1+WLS0 ; UART FORMAT (8 DATA,

0020 = BAUDRAT EQU BAUD48 ; CURRENT BAUD RATE ; NO PARITY)
 00FF = CUSHION EQU 255 ; THE MINIMUM NUMBER OF BYTES ; AVAILABLE IN THE TERMINAL BUFFER THAT ; ARE REQUIRED BEFORE A RECEIVE ; OPERATION IS STARTED.
 2710 = ACKTO EQU 10000 ; ACKNOWLEDGE TIMEOUT COUNT ; (PRELIMINARY VALUE)

 0800 ORG 800H ; THIS PROGRAMS EPROM START ADR.
 ; ENTRY JUMP TABLE
 0800 C31508 JMP TJPINIT ; INITIALIZATION ENTRY POINT
 0803 C34808 JMP RST55 ; INTERRUPT FROM 8250
 0806 C30608 JMP \$; UNUSED INTERRUPT ENTRY POINT
 0809 C3100A JMP DISPRX ; TO DISPATCHER ROUTINE
 080C OC17564537RIMBUF DB 12,RIMD,'VE7APU' ; CONNECT BUFFER TERMNO DB 200 ; THIS NODES TERMINAL NUMBER
 0814 C8 *****
 TIPINIT:
 ; SET BAUD RATE IN SERIAL PORT
 MVI A,DLAB
 OUT LCR
0819 3E20 MVI A,LOW BAUDRAT
 OUT DLL ; BAUD RATE DIVISOR LSB
 MVI A,HIGH BAUDRAT ; BAUD RATE DIVISOR MSB
 OUT DLM ; BAUD RATE DIVISOR MSB
 ; DEFINE CHARACTER FORMAT OF SERIAL DATA
 MVI A,FORMAT
 OUT LCR ; UPDATE LINE CONTROL REGISTER
 ; UNMASK INTERRUPTS FROM SERIAL INTERFACE
 RIM 20H ; GET CURRENT INTERRUPT MASK IN A
 DB 000000110B ; READ INTERRUPT MASK
 AN1 000000110B ; RESET RST5.5 MASK BIT
 OR1 MSE ; SET MASK SET ENABLE BIT
 SIM ; ENABLE RST5.5 INTERRUPTS
 DB 30H ; SET INTERRUPT MASK
 ; CLEAR OUT RECEIVE BUFFER REGISTER
 IN RBR
 ; SET UP INITIAL DISPATCH ROUTINES
 LX1 H,EXIT ; SET RECEIVE INTERRUPT TO IDLE
 SHLD RNEXT
 LX1 H,WAITLIP ; WAITING FOR LIP BLOCK
 SHLD TDISP
 LXI H,WAITTB ; WAITING FOR FREE CUSHION
 SHLD RDISP
 ; ENABLE RECEIVED DATA AVAILABLE AND MODEM STATUS INTRPT
 MVI A,ERBFI+EDSSI ; RECEIVE AND MODEM
 OUT IER ; UPDATE INTERRUPT REGISTER
 ; BRING UP RLSD (OUT1 = RLSD)
 MVI A,OUT1
 OUT MCR ; UPDATE MODEM CONTROL REGISTER
 ; RETURN TO LIP FOR COMPLETION OF INITIALIZATION
 RET

 0848 F5 RST55: PUSH PSW
 0849 E5 PUSH H
 084A D5 PUSH D
 084B C5 PUSH B
 084C DB02 IN IIR ; GET INTERRUPT IDENT INFORMATION
 084E FE04 CPI IID1 ; RECEIVED DATA AVAILABLE INTRPT?
 0850 CA8A08 JZ RXINT ; GO TO RECEIVE INTERRUPT ROUTINE

0853 FE02 CPI 1100 ; IS IT TRANSMIT BUFFER EMPTY
 0855 CA4909 JZ TXINT ; GO TO TRANSMIT INTRPT ROUTINE
 0858 B7 ORA A ; MODEM STATUS INTERRUPT?
 0859 CA5F08 JZ MSINT ; TO MODEM STATUS INTRPT ROUTINE
 085C C34309 JMP EXIT ; UNKNOWN INTERRUPT, RETURN
 085F DB06 MSINT: IN MSR ; GET MODEM STATUS
0861 324210 STA MSRSAVE ; SAVE MODEM STATUS FOR DISPATCH
 0864 4F MOV C,A ; SAVE IT
 0865 E601 AN1 DCTS ; HAS CTS CHANGED?
 0867 C46D08 CNZ CTSINT ; YES GO HANDLE CTS CHANGE
 086A C34309 JMP EXIT
 086D 79 CTSINT: MOV A,C ; GET MODEM STATUS BACK
 086E E610 AN1 CTS ; TEST CTS BIT
0870 CA7608 JZ DISABLETX ; OFF, DISABLE TRANSMIT
 0873 C37D08 JMP ENABLETX ; TRY TO ENABLE TRANSMIT
 0876 DB01 DI SABLETX: IN IER ; GET INTERRUPT ENABLE REGISTER
 0878 E6FD AN1 OFFH-ETBEI ; TURN OFF TRANSMIT INTERRUPTS
 087A D301 OUT IER ; TURN OFF TRANSMIT INTERRUPTS
 087C C9 RET
 087D 3A4310 ENABLETX: LDA INTFLAG ; IS TRANSMITTER BUSY?
 0880 E602 ANI TXBUSY
 0882 C8 RZ
 0883 DB01 IN IER ; GET INTERRUPT ENABLE REGISTER
0885 F602 OR1 ETBEI
0887 D301 OUT IER ; ENABLE TRANSMIT INTERRUPTS
 0889 C9 RET
 088A DB00 RXINT: IN RBR ; READ DATA FROM SERIAL PORT
088C 2A4A10 LHLD RNEXT ; GO TO ROUTINE ADDRESS IN RNEXT
 088F E9 PCHL
 0890 FE10 RSTART: CPI DLE ; IS IT A DATA LINK ESCAPE?
 0893 C24309 JNZ EXIT ; NO
 0895 219E08 LX1 H,RSTX ; YES, NOW WAIT FOR START OF TEXT
 0898 224A10 SHLD RNEXT
 089B C34309 JMP EXIT
 089E FE02 RSTX: CPI STX ; IS IT START OF TEXT
 08A0 C2AC08 JNZ RSTX1 ; NO
 08A3 21B508 LX1 H,RDATA ; YES, HANDLE TRANSPARENT DATA
 08A6 224A10 SHLD RNEXT
 08A9 C34309 JMP EXIT
08AC 219008 RSTX1: LX1 H,RSTART ; FALSE START GO BACK
 08AF 224A10 SHLD RNEXT ; TO BEGINNING
 08B2 C34309 JMP EXIT
 08B5 FE10 RDATA: CPI DLE ; IS IT A DLE?
 08B7 CAC308 JZ RDATA1 ; YES
 08BA CDEE08 CALL RPUT ; NO, PUT DATA INTO BUFFER
 08BD CA0609 JZ RESTART ; ERROR, RESET BUFFER AND RESTART
 08C0 C34309 JMP EXIT ; FROM BEGINNING
 08C3 21CC08 RDATA1: LX1 H,RCONTROL ; RECEIVE CONTROL
 08C6 224A10 SHLD RNEXT ; CHARACTER NEXT
 08C9 C34309 JMP EXIT
 08CC FE10 RCONTROL: CPI DLE ; IS IT A SECOND DLE?
 08CE C2E008 JNZ RCONTROL1 ; NO, CHECK FOR ETX
 08D1 CDEE08 CALL RPUT ; YES, PUT DLE IN BUFFER
 08D4 CA0609 JZ RESTART ; ERROR, RESET BUFFER AND RESTART
 08D7 21B508 LX1 H,RDATA ; GO BACK FOR MORE DATA
 08DA 224A10 SHLD RNEXT
 08DD C34309 JMP EXIT
 08E0 FE03 RCONTROL1: CPI ETX ; IS IT END OF TEXT?

08E2 C20609 08E5 211D09 08E8 224A10 08EB C34309	JNZ LXI RESTART ; NO, ERROR - RESTART H,R1CRC ; NEXT RECEIVE FIRST CRC CHAR SHLD RNEXT JMP EXIT	0969 D300 096B 217409 096E 224C10 0971 C34309	OUT THR H,TDATA ; NEXT FUNCTION HANDLES TEXT DATA LX1 TNEXT SHLD JMP EXIT
08EE 4F RPUT: MOV C,A ; SAVE DATA IN REGISTER C LHLD OTBE ; PUT DATA INTO BUFFER	0974 211D10	TDATA: LXI H,OUTCOUNT ; MORE DATA IN BUFFER? MOV A,M ORA A JZ TDATA1 ; NO, BUFFER EMPTY	
08EF 2A0610 08F2 EB 08F3 2A0810	XCHG LHLD TBIP 1 INCTB MVI A,1 2 RZ ; RETURN WITH ZERO STATUS IF OVERFLOW SHLD TBIP ; UPDATE POINTER IF OK MOV M,C ; MOVE DATA INTO BUFFER LX1 H,BUFCOUNT ; INCREMENT COUNT OF DATA	0979 CA9709 097C 35 097D 2A1A10	DCR M LHLD LBOP INCLB A,1 3 RST SHLD LBOP ; LBOP = LBOP+1
08F6+3E01 08F8+D7 08F9 C8 08FA 220810 08FD 71 08FE 211C10 0901 34 0902 7E 0903 FEFB 0905 C9	MVI INR M MOV A,M CPI 251 ; HAVE WE GOT 251 BYTES NOW? RET ; ZERO STATUS IF TOO MANY BYTES	0980+3E01 0982+DF 0983 221A10 0986 7E 0987 D300 0989 FE10 098B C24309 098E 21A409 0991 224C10	CPI DLE ; IS IT SAME AS DLE? JNZ EXIT ; NO LXI H,TDLE ; TRANSMIT ANOTHER DLE SHLD TNEXT ; TO MAKE TRANSPARENT JMP EXIT
0906 3E00 0908 321C10 090B 2A0410	RESTART: MVI A,0 ; SET COUNT IN BUFFER TO ZERO STA BUFCOUNT LHLD CTBIE 1 ; SET INPUT POINTER JUST BEFORE INCTB DATA AREA	0994 C34309 0997 3E10 0999 D300 099B 21B109 099E 224C10 09A1 C34309	TDATA1: MVI A,DLE ; OUTPUT A DATA LINK ESCAPE OUT THR H,TETX ; NEXT SEND END OF TEXT LXI H,TETX ; AND GO BACK TO TRANSPARENT MODE
090E+3E01 0910+D7 0911 220810 0914 219008 0917 224A10 091A C34309	MVI RST 2 SHLD TBIP LX1 H,RESTART ; AND RESTART RECEIVER RNEXT JMP EXIT	09A4 3E10 09A6 D300 09A8 217409 09AB 224C10 09AE C34309	TDLE: MVI A,DLE ; SEND DATA LINK ESCAPE OUT THR H,TDATA ; AND GO BACK TO TRANSPARENT MODE
091D 324710 R1CRC: STA RCRC1 ; SAVE FIRST CRC CHARACTER 0920 212909 LX1 H,R2CRC ; NOW GET SECOND CRC CHARACTER 0923 224A10 SHLD RNEXT 0926 C34309 JMP EXIT	09B1 3E03 09B3 D300 09B5 21BE09 09B8 224C10 09BB C34309	TETX: MVI A,ETX ; SEND END OF TEXT OUT THR H,T1CRC ; NEXT SEND FIRST CRC CHARACTER	
0929 324610 R2CRC: STA RCRC2 ; SAVE SECOND CRC CHARACTER 092C DB04 MCR ; RESET REQUEST TO SEND 092E E6FD AN1 OFFH-RTS 0930 D304 OUT MCR 0932 3A4310 LDA INTFLAG ; INDICATE RECEIVE ROUTINE 0935 E6FE AN1 OFFH-RXBUSY ; IS NOT ACTIVE 0937 324310 STA INTFLAG 093A 214309 LX1 H,EXIT ; IGNORE ALL RECEIVE INTERRUPTS 093D 224A10 SHLD RNEXT 0940 C34309 JMP EXIT	09BE 3A4910 09C1 D300 09C3 21CC09 09C6 224C10 09C9 C34309	T1CRC: LDA TCRC1 ; SEND FIRST CRC CHARACTER OUT THR H,T2CRC ; NEXT SEND SECOND CRC CHARACTER	
0943 C1 EXIT: POP B 0944 D1 POP D 0945 E1 POP H 0946 F1 POP PSW 0947 FB EI 0948 C9 RET	09CC 3A4810 09CF D300 09D1 21DA09 09D4 224C10 09D7 C34309	T2CRC: LDA TCRC2 ; SEND SECOND CRC CHARACTER OUT THR H,TPAD ; SEND TRAILING PAD CHARACTER	
***** ; TRANSMIT INTERRUPT ROUTINES	09DA 3EFF 09DC D300 09DE 3A4310 09E1 E6FD 09E3 324310 09E6 CD7608 09E9 C34309	TPAD: MVI A,PAD ; SEND TRAILING PAD AFTER CRC OUT LDA INTFLAG ; MARK TRANSMIT NOT BUSY AN1 OFFH-TXBUSY STA INTFLAG CALL DISABLETX JMP EXIT	
0949 2A4C10 TXINT: LHLD TNEXT ; DISPATCH ADDRESS IN TNEXT 094C E9 PCHL	09EC F5 09ED 0608 09EF 4F 09F0 2A4410 09F3 = 09F3 79 09F4 07 09F5 4F 09F6 7D 09F7 17	***** ; CRC CALCULATION ROUTINE ; INCLUDES BYTE IN ACCUMULATOR IN CRC CALCULATION CALCCRC: PUSH PSW MOV B,8 MOV C,A LHLD CRC CALCCRC1: EQU \$ MOV A,C RLC MOV C,A MOV A,L RAL	
0940 3E16 TSTART: MVI A,SYN ; OUTPUT A SYN CHARACTER 094F D300 OUT THR 0951 215A09 LX1 H,TDLE1 ; NEXT SEND A DLE 0954 224C10 SHLD TNEXT 0957 C34309 JMP EXIT	09F8 0608 09F9 4F 09F0 2A4410 09F3 = 09F3 79 09F4 07 09F5 4F 09F6 7D 09F7 17		
095A 3E10 TDLE 1: MVI A,DLE ; OUTPUT A DLE 095C D300 OUT THR 095E 216709 LXI H,TSTX ; NEXT OUTPUT START OF TEXT 0961 224C10 SHLD TNEXT 0964 C34309 JMP EXIT			
0967 3E02 TSTX: MVI A,STX ; OUTPUT START OF TEXT			

2.45

<pre> 09F8 6F MOV L,A 09F9 7C MOV A,H 09FA 17 RAL H,A 09FB 67 MOV CALCRC2 09FC D2070A JNC A,H 09FF 7C MOV 80H 0AO0 EE80 XRI H,A 0AO2 67 MOV A,L 0AO3 7D MOV A,L 0AO4 EE05 XRI 05H 0AO6 6F MOV L,A 0AO7 = CALCRC2: EQU \$CALCRC2 0AO7 05 DCR B 0AO8 C2F309 JNZ CALCRC1 0AOB 224410 SHLD CRC 0AOE F1 POP PSW 0AOF C9 RET ***** ; RECEIVE SIDE DISPATCH ROUTINES </pre> <p>0A10 2A4E10 DISPRX: LHLD RDISP ; GO TO RECEIVE DISPATCH ROUTINE</p> <p>0A13 E9 PCHL</p> <p>0A14 2A0610 WAITTB: LHLD OTBE ; TERMINAL BUFFER CUSHION FREE?</p> <p>0A17 EB XCHG</p> <p>0A18 2A0410 LHLD COMPARE ; COMPARE DE TO HL</p> <p>0A1B+EF RST 5 ;</p> <p>0A1C CA280A JZ WAITTB1 ; SAME, BUFFER AVAILABLE</p> <p>0A1F+3EFF INCTB CUSHION ; IS CUSHION FREE?</p> <p>0A21+D7 MVI A,CUSHION</p> <p>0A22 DA120B JC DISPTX ; TO TRANSMIT ROUTINE DISPATCHER</p> <p>0A25 2A0410 LHLD CTBIE ; POINT TBIP JUST AHEAD OF DATA</p> <p>0A28+3E01 WAITTB1: INCTB 1</p> <p>0A2A+D7 MVI A,1</p> <p>0A2B 220810 RST 2</p> <p>0A2E 3E00 SHLD TBIP</p> <p>0A30 321210 MVI A,0 ; ZERO COUNT FOR RECEIVE ROUTINE</p> <p>0A33 F3 BUFCOUNT</p> <p>0A34 3A4310 LDA INTFLAG ; RECEIVE ROUTINE IS ACTIVE</p> <p>0A37 F601 OR1 RXBUSY</p> <p>0A39 324310 STA INTFLAG</p> <p>0A3C FB EI</p> <p>0A3D 219008 LX1 H,RESTART ; START RECEIVING</p> <p>0A40 224A10 SHLD RNEXT</p> <p>0A43 DB04 IN MCR ; SET RTS SO OTHER END WILL SEND</p> <p>0A45 F602 OR1 RTS</p> <p>0A47 D304 OUT MCR</p> <p>0A49 21500A LX1 H,WAITRX ; WAIT FOR BLOCK</p> <p>0A4C 224E10 SHLD RDISP</p> <p>0A4F C9 RET</p> <p>0A50 3A4310 WAITRX: LDA INTFLAG ; IS RECEIVER STILL BUSY?</p> <p>0A53 E601 AN1 RXBUSY</p> <p>0A55 C2120B JNZ DISPTX ; YES, GO TO TRANSMIT DISPATCHER</p> <p>0A58 3A5210 LDA DFLAG ; GET DISPATCHER FLAG</p> <p>0A5B E601 AN1 CRCTX ; IS CRC ROUTINE BUSY?</p> <p>0A5D C2120B JNZ DISPTX ; YES, GO TO TRANSMIT DISPATCHER</p> <p>0A60 211C10 LX1 H,BUFCOUNT ; COUNT OF BYTES RECEIVED</p> <p>0A63 7E MOV A,M</p> <p>0A64 2A0410 LHLD CTBIE ; POINT TO CURRENT INPUT ENTRY</p> <p>0A67 77 MOV M,A ; PUT COUNT IN BUFFER HEADER</p> <p>0A68+3E01 INCTB 1 ; POINT JUST BEFORE DATA AREA</p> <p>0A6A+D7 MVI A,1</p> <p>0A6B 220810 RST 2</p> <p>0A6E 210000 SHLD TBIP</p> <p>0A71 224410 LX1 H,0 ; INITIALIZE CRC VALUE</p> <p>0A74 217B0A SHLD CRC</p> <p>0A77 224310 LX1 H,RXCRC ; NEXT CALCULATE CRC</p> <p>SHLD RDISP</p>	<pre> 0A7A C9 RET 0A7B 211C10 RXCRC: LXI H,BUFCOUNT ; MORE DATA TO INCLUDE? 0A7E 7E MOV A,M 0A7F B7 ORA A 0A80 CA970A JZ RXCRC1 ; NO, GO TO INCLUDE CONTROL CHARS 0A83 35 DCR M ; DECREMENT COUNT 0A84 2A0810 LHLD TBIP ; UPDATE POINTER TO NEXT POSITION 1 0A87+3E01 INCTB 0A89+D7 MVI A,1 0A8A 220810 RST 2 0A8D 7E SHLD TBIP 0A8E CDEC09 MOV A,M ; GET DATA BYTE IN A 0A91 FE10 CALL CALCCRC ; INCLUDE IT IN CRC CALCULATION 0A93 CCEC09 CPI DLE ; WAS IT DATA LIKE A DLE? 0A96 C9 CZ CALCCRC ; DO ANOTHER FOR TRANSPARENCY 0A97 3E10 RET / RETURN TO LIP 0A99 CDEC09 RXCRC1: MVI A,DLE ; INCLUDE DLE AND ETX IN CRC 0A9C 3E03 CALL CALCCRC 0A9E CDEC09 MVI A,ETX 0AA1 21A80A CALL CALCCRC 0AA4 224E10 LXI H,CHECKCRC ; NEXT CHECK THE CRC 0AA7 C9 SHLD RDISP ; GO INCLUDE CRC CHARS RECEIVED RET </pre> <p>0AA8 3A4710 CHECKCRC: LDA RCRC1 ; INCLUDE RECEIVED CRC CHARACTERS</p> <p>0AAB CDEC09 CALL CALCCRC</p> <p>0AAE 3A4610 LDA RCRC2</p> <p>0AF1 CDEC09 CALL CALCCRC</p> <p>0AB4 21BB0A LXI H,CHKFIN ; NEXT CHECK IF CRC IS GOOD</p> <p>0AB7 224310 SHLD RDISP</p> <p>0ABA C9 RET</p> <p>0ABB 2A4410 CHKFIN: LHLD CRC ; GET CALCULATED CRC</p> <p>0ABE 7D MOV A,L ; IS IT ZERO?</p> <p>0ABF B4 ORA H</p> <p>0AC0 C2D00A JNZ CHKFIN1 ; NO, GO RESTART RECEIVE OPERATION</p> <p>0AC3 DB04 IN MCR ; YES, GOOD CRC, FLIP DTR</p> <p>0AC5 EE01 XRI</p> <p>0AC7 D304 OUT MCR</p> <p>0AC9 21D70A LXI H,RPROC ; PROCESS CHECKED BLOCK</p> <p>0ACC 224310 SHLD RDISP</p> <p>0ACF C9 RET</p> <p>0ADO 21140A CHKFIN1: LXI H,WAITTB ; BAD CRC, TRY AGAIN</p> <p>0AD3 224E10 SHLD RDISP</p> <p>0AD6 C9 RET</p> <p>0AD7 2A0410 ; THIS ROUTINE SHOULD PROCESS THE BUFFER PREFIX</p> <p>0ADA 7E ; TEMPORARILY IT ONLY PASSES THE BUFFER TO THE LIP</p> <p>0ADB FE07 ; AND HANDLES CONNECT/DISCONNECT</p> <p>0ADD DA020B RPROC: LHLD CTBIE ; IS COUNT 7 OR MORE?</p> <p>0AE0+3E08 MVI A,M</p> <p>0AE2+D7 RST 7</p> <p>0AE3 7E MOV A,M ; DISCONNECT</p> <p>0AE4 FE01 CPI 'A'-40H ; IS IT CONNECT?</p> <p>0AE6 C2F30A JNZ RPROC1 ; NO, GO TO TEST FOR DISCONNECT</p> <p>0AE9 3E00 MVI A,0 ; O FOR CONNECT</p> <p>0AEB F7 RST 6 ; COMMUNICATE REQUEST TO LIP</p> <p>0AEC 21140A LXI H,WAITTB ; DON'T PASS THIS ENTRY</p> <p>0AEE 224E10 SHLD RDISP</p> <p>0AF2 C9 RET</p> <p>0AF3 FE02 RPROC2: CPI 'B'-40H ; IS IT DISCONNECT?</p> <p>0AF5 C2020B JNZ RPROC2 ; NO, PASS TO LIP</p> <p>0AF8 3E01 MVI A,1 ; YES, 1 FOR DISCONNECT</p> <p>0AFA F7 RST 6 ; COMMUNICATE REQUEST TO LIP</p> <p>0AFC 21140A LXI H,WAITTB ; DON'T PASS THIS ENTRY</p> <p>0AFE 224310 SHLD RDISP</p> <p>0B01 C9 RET</p>
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0B02 2A0810	RPROC2: LHLD TBIP ; UPDATE CURRENT INPUT ENTRY	0B85 325210 0B88 214D09 0B8B 224C10 0B8E 2A1610 0B91 7E 0B92 321D10	STA DFLAG ; DSR IN DFLAG LX1 H,TSTART ; SET UP INITIAL XMIT SHLD TNEXT ; INTERRUPT ROUTINE LHLD OLBE ; POINT TO DATA TO TRANSMIT MOV A,M ; GET COUNT STA OUTCOUNT INCLB 3 MVI A,3 RST 3 SHLD LBOP
0B05+3E01	MVI A,1	0B95+3E03 0B97+DF	DI INTFLAG ; DISABLE INTERRUPTS LDA INTFLAG ; INDICATE TRANSMIT BUSY
0B07+D7	RST 2	0B98 221A10 0B9B F3 0B9C 3A4310 0B9F F602 0BA1 324310	OR1 TXBUSY STA INTFLAG LDA MSRSAVE ; IS CTS UP? AN1 CTS JZ STARTTX1 ; DON'T ENABLE TRANSMIT INTRPT IN IER ; YES, ENABLE TRANSMIT INTERRUPTS
0B08 220410	SHLD CTBIE	0BA4 3A42 10 0BA7 E610 0BA9 CAB20B 0BAC DB01 0BAE F602	OR1 ETBEI OUT IER
0B0B 21140A	LX1 H,WAITTB ; NOW GO GET ANOTHER ONE	0BB0 D301 0BB2 FB 0BB3 21BA0B 0BB6 225010 0BB9 C9	STARTTX1: EI LX1 SHLD RET
0B0E 224E10	SHLD RDISP	OBBA 3A4310 OBBD E602 OBBF C0 0BC0 211027 0BC3 224010	WAITTX: LDA INTFLAG ; TRANSMITTER INTERRUPTS ENABLED? ANI TXBUSY RNZ
0B11 C9	RET	0BC6 21CDOB 0BC9 225010 OBCC C9	OR1 ; YES, RETURN H,ACKTO ; NO, SET UP FOR TIMEOUT WAIT ; INITIALIZE ACKNOWLEDGE TIMEOUT H,WAITACK ; NEXT WAIT FOR ACKNOWLEDGE TDISP
0B12 2A5010	DISPTX: LHLD TDISP ; GO TO TRANSMIT DISPATCH ROUTINE	OBDA 215210 OBDD 3A4210 OBD3 AE OBDA E620 OBDD 2A4010 OBDC 2B OBDD 224010 OBEE 7C OBEB 1B5 OBEC C0 OBED 217908 OBEE 225010 OBEE9 C9	WAITACK: LX1 MSRSAVE LDA M XRA DSR JNZ WAITACK1 ; NO, BLOCK ACKNOWLEDGED LHLD WAIT ; YES, DECREMENT TIMEOUT COUNT DCX H SHLD WAIT MOV A,H ; IS TIME OVER? RNZ L OR1 ; NO, RETURN L,STARTTX ; YES, TIMED OUT, SO SEND AGAIN SHLD TDISP
0B15 E9	;	OBEB 21160B OBED 225010 OBFO C9	END
0B16+E7	RST 4	OBFF1	H,WAITLIP ; GOOD ACK, GET ANOTHER BUFFER TDISP ; FROM LIP
0B17 C8	RZ		
0B18 3A5210	LDA DFLAG ; INDICATE TX SIDE USING CRC		
0B1B F601	OR1 CRCTX ; ROUTINES		
0B1D 325210	STA DFLAG		
0B20 7E	MOV A,M ; GET DATA LENGTH FROM HEADER		
0B21 321D10	STA OUTCOUNT ; FOR CRC CALCULATION ROUTINE		
0B24+3E03	INCLB 3 ; POINT JUST BEFORE DATA AREA		
0B26+DF	MVI A,3		
0B27 221A10	RST 3		
0B2A 210000	SHLD LBOP ; FOR CRC CALCULATION ROUTINE		
0B2D 224410	LX1 H,0 ; INITIALIZE CRC VALUE		
0B30 21370B	SHLD CRC		
0B33 225010	LX1 H,TXRC ; NEXT START CRC CALCULATION		
0B36 C9	SHLD TDISP		
0B37 211D10	RET		
0B3A 7E	TXCRC: LXI H,OUTCOUNT ; ANY MORE DATA TO INCLUDE?		
0B3B B7	MOV A,M		
0B3C CA530B	ORA A		
0B3F 35	JZ TXC RC 1 ; NO, GO TO INCLUDE CONTROL CHARS		
0B40 2A1A10	DCR M ; DECREMENT COUNT		
0B43+3E01	LHLD LBOP ; UPDATE POINTER TO NEXT POSITION		
0B45+DF	INCLB 1		
0B46 221A10	MVI A,1		
0B49 7E	RST 3		
0B4A CDEC09	SHLD LBOP		
0B4D FE10	MOV A,M ; GET DATA BYTE IN A		
0B4F CCEC09	CALL CALCCRC ; INCLUDE IT IN CRC CALCULATION		
0B52 C9	CPI DLE ; WAS IT DATA LIKE A DLE?		
0B53 3E10	CZ CALCCRC ; DO ANOTHER FOR TRANSPARENCY		
0B55 CDEC09	RET ; RETURN TO LIP		
0B58 3E03	TXCRC1: MVI A,DLE ; INCLUDE DLE AND ETX IN CRC		
0B5A CDEC09	CALL c ALC c RC		
0B5D 21640B	MVI A,ETX		
0B60 225010	CALL CALCCRC		
0B63 C9	LXI H,CRCFIN ; NEXT TO FINISH CRC FOR SENDING		
0B64 3E00	SHLD TDISP		
0B66 CDEC09	CRCFIN: MVI A,0 ; FINISH OFF CRC CALCULATION FOR		
0B69 CDEC09	CALL CALCCRC ; TRANSMISSION		
0B6C 2A4410	CALL CALCCRC		
0B6F 224810	LHLD CRC ; SAVE CALCULATION FOR TRANSMIT		
0B72 21790B	SHLD TCR2		
0B75 225010	LX1 H,STARTTX ; NEXT, START TRANSMITTING		
0B78 C9	SHLD TDISP ; THE BLOCK		
0B79 3A4210	RET		
0B7C E620	STARTTX:LDA MSRSAVE ; SAVE CURRENT DSR LEVEL		
0B7E 67	AN1 DSR		
0B7F 3A5210	MOV H,A		
0B82 E6DE	LDA DFLAG		
0B84 B4	AN1 OFFH-CRCTX-DSR ; INDICATE CRC ROUTINE		
	ORA H ; NOT IN USE AND SAVE		