THE EASTNET NETWORK CONTROLLER

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Abstract

This paper describes a proposed packet radio network control computer running at high packet baud rates on the East Coast Amateur Packet Network, EASTNET. Principally discussed is the digital hardware, but also mentioned is some crude RF hardware to accompany the control computer. The digital side uses STD bus hardware developed by Jon Bloom, KE3Z to begin testing, and eventually will use the AMRAD Packet Assembler Disassembler (PAD) board running in an S-100 Bus (IEEE-696) computer.

Introduction

The basis of a real packet radio network is the packet switch, which in its simplest implementation is a two port HDLC I/O board running in a microcomputer.

A Z80 based, STD bus computer has been assembled which is capable of sending and receiving high speed packets, of at least 48K bits/second and possibly 56K bits/second. This computer can form the basis of the network controller, the smart packet switch. It will first be tested on a wire connecting two such devices.

After the packet switch digital hardware is tested, running at some high speed, the required RF hardware must be constructed. Work will begin at 9600 baud, using already proven technology designed by Stan Kazmiruk, VE3JBA. After duplicating Stan's system, the hardware can be upgraded to faster speeds, at least as fast as the digital hardware.

Following the successful testing of the packet switch, the current in-place 1200 baud repeaters can be replaced with the new equipment, thus increasing the thruput.

Background

The essential element of network hardware is the digital packet switch. In the crude kludge, a packet is received containing multiple repeater addresses and the network hardware consists of a repeater which accepts the packet, checks it for correctness (CRC correct), looks for its address somewhere in the repeater fields (up to 8 fields currently allowed), and upon finding its address, the packet is repeated, after setting an agreed upon "has been repeated bit".

A slow network can be constructed with this simple protocol, but it will not meet the design goal of coast to coast packet connections. The real network controller is a true two port syncronous HDLC device that sends and receives packet traffic on both ports simultaneously. More to the point of this paper, it does it quickly (higher baud rate than the local area networks it serves). To achieve our design goal, we require a real IS0 Level 3 protocol with the software for it implemented in our network packet switch. I am leaving the protocol fight to others and intend to provide fast hardware to implement whatever is agreed upon.

Existing Hardware

The Vancouver Digital Communication Group Terminal Node Controller board is currently being used to communicate on the local area networks around the country at 1200 baud. It will not go much faster on the packet side due to the slow clock speed, the noisy 74LS138 I/O decoder and slow 2708 EPROMs. Bill Ashby has been trying to get it to function at 9600 baud and has failed.

The Tucson Amateur Packet Radio (TAPR) terminal node controller may go higher speeds than 1200 baud by not using the on board modem and cranking up the clock speed. However, Tom Clark, W3IWI says the interrupt structure may be overrun at 9600 baud. This represents an unknown at this point. There appears no way to go 48K bit/second or greater speed.

The Bill Ashby terminal node controller has been tested at 9600 baud and works well. It probably will not go faster than that, but Bill is testing it.

The AMRAD Packet Assembler Disassembler (PAD) board, designed by Terry Fox, WB4JFI, exists only as a prototype board currently with plans for making printed circuit boards sometime in the future. It is not available for high speed experimentation, but will be capable of the higher speeds once it is in production.

An STD bus packet radio repeater exists and can possibly be used for high speed work. AMRAD is proceeding along these lines. The repeater is currently working and requires little modification to be used in network service.

STD Blue Box Description

The STD bus was developed commercially by PRO-LOG, and is supported by over 30 manufacturers including MOSTEK. AMRAD managed to obtain some STD computers (referred to as the "Blue Box") at a reasonable price. The computers used the MOSTEK MDX-CPU2 CPU card, a Z80 microprocessor with on board Counter/Timer (CTC) circuit and RAM/ROM sockets for 11K of memory. The heart of the packet work is accomplished with the MDX-SIO Serial I/O module, a serial board based on the Z80 SIO controller. The STD Bus is not the integral part of this system, the SIO is. This hardware could have been placed on the S-100 Bus just as simply. In fact, the designer of this packet project (Jon Bloom, KE3Z) has done just that,, using the California Computer systems CPU card containing an SIO and CTC, however no details of that work are available and the CPU card price is excessive.

The problem with using a Z80 SIO is that it does not do digital phase lock loop (DPLL) recovery of the data derived clock, nor does it do NRZI encoding. Jon solved this problem 'by building a state machine (prom and latch!) for receive and another for transmit to perform these functions. Details of this design (what is in the proms and schematic) is available from the AMRAD Corresponding Secretary. Using this hardware!, repeater software was written to use this box as a digital repeater. This repeater functions well at 1200 baud while connected to a conventional Bell Standard 202 modem. This box thus forms the basis of the big experiment.

Proposed Experimentation with Digital Hardware

The proposed experinnentation will begin with the construction of a second STD box to hook to the first with a standard RS232 wire cable. The jumpers on the SIO cards are first set at 1200 baud. The current software repeats, but is modular. A short bit of additional software can be easily written to send a packet from Box 1 to Box 2 (running the repeater software). Box 2

will repeat the packet and send it back to Box 1, which will receive it and display it on the system console. Then, the jumpers are moved in both boxes to run successively higher speeds until a packet is no longer returned.

Jon's estimate is that 48 K bits/second is going to work fine, but 56K bits/second may prove a problem.

Another possible upgrade could be made to the STD hardware with a little effort. The SIO board and state machine board could both be replaced with a 8530 Serial Communications Controller (SCC) board. This is the same chip used on the AMRAD PAD board. A kludge board has been purchased for this purpose. This makes good sense as software could be easily developed in the STD box and transferred to the PAD board with few changes. This would be actually easy as very few support chips should be required to put the 8530 on the STD bus. No state machines would be required as the 8530, like the 8273 and 1933, performs the required DPLL and NRZI functions.

Another additional benefit could be derived by keeping the old SIO board around. Two independent channels of HDLC could be run, thus achieving our true network control easily. The only drawback is the required development time as the SIO-State Machine board works now.

Assume for the sake of discussion that 48K bits/second works properly. Then, RF boxes is the next logical step. The jumpers can be returned to 9600 baud and proceed to the next step.

Proposed Experimentation with RE Hardware

Several years ago, Stan Kazmiruk, VE3JBA, published the designs for the Ottawa Digipeater. This hardware repeated 9600 baud packets using a transmitted signal with modulation of +/- 2.5 KHz which proved to be 12 to 14 KHz wide at 6 db down and not over 22 KHz wide at 30 db down. The design centered around transmitter and receiver modules made by VHF Engineering, a company no longer making these modules. Stan mentioned that Hamtronics was making similar modules that should work. AMRAD has a number of these modules and are now testing them for this high speed work. They appear to be capable of 4800 baud as they are shipped and perhaps greater by disconnecting some crystal filter stages. The principal is clear and is receiving attention in New Jersey also (Bill Ashby's gang are going 9600 baud now). Transmit is done by direct FSK of the transmitter, and place the demodulator at the IF (10.7MHz or 455KHz). Faster speeds are certainly possible. Video techniques should get us to 56K bits/second.

Conclusion

The low speed 1200 baud packet work going on all over the country now is fine for local area work. Higher speeds are required for networking. The hardware/software needed for networking need not be copied by a causual observer as the network packet switch is much more complicated than a TAPR board and not as many are required. We should set our sights at going as high a speed as our allowed 100KHz bandwidth will allow. We should use 220MHz for this work as it is relatively unused over the majority of the country and needs to be saved from the commercial land mobile radio service.