A HIGH PERFORMANCE PACKET SWITCH

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This paper describes the PS-186™, a high-speed multiport packet switch designed to support data rates up to 1 Mbit/second. It can also be used as a local packet node, mail system, or a gateway to other networks. It operates on 2.1 Watts of power. The PS-186 was designed by members of the San Diego Packet Radio Association (SANDPAC).

WHY WE BUILT IT

As requirements grow, existing packet radio hardware is running out of steam.

We believe the advancement of amateur packet radio requires packet switch hardware which will support data rates far in excess of today's standard 1200 bit/second links. While 1200 bit/second easily supports one typed conversation between two individuals, packet radio channels are shared channels, and must support many users simultaneously. To operate without congestion, the channel data rate must be many times higher than the rate desired by an individual user. Growing computer-to-computer communication is also creating a demand for higher user data rates. A more reasonable data rate for local area channels is 56 kb/s, with much higher rates, possibly 1 Mb/s, on the backbone.

A typical mountaintop requirement might be two 1 Mb/s ports (for point-to-point links to other mountaintops, say one North, one South), a 56 kb/s local radio port (connectivity to individual users), and a 1200 b/s local radio port (for connectivity with the TNC 1&2 community). With such applications in mind, we set forth to build a four-port packet switch capable of operation to 1 Mb/s.

DESIGN CONSIDERATIONS

The switch should provide a very flexible modem interface. Compatibility with existing modem designs was a must, but the modems we hope to use with this device haven't been designed yet! (There are promising developments, such as the WA4DSY *56* kb/s modem.) We don't know what data rates will become standard, and some modems will want to generate their own clocks, so the ports must have external clock options. We wanted to support modems that derive their own RX bit timing as well as those that do not, async as well as HDLC link-level protocols, etc.

Processors on existing packet hardware are running out of address space to hold sophisticated protocol software, and never really had the capacity to handle high data rate operations. We wanted a processor with more address space, more speed, and a large installed base, so that as many people as possible would have access to development tools. Because remote packet switch locations might be battery operated, the processor and all support circuitry should be available in CMOS versions. The solution was an Intel 80186 processor, running at 8 MHz[1], with no wait states, and full DMA[2] support. This processor, except for low-level I/O functions accessed only by I/O drivers, is software compatible with the IBM PC, IBM AT, and their clones, which now have an installed base of over *IO million units.* More sophisticated processors were considered, but none are available at as low a cost, or require as few support chips as the 186.

We felt that developers of complex packet-switch software should have the capability of loading new software into packet switches remotely. This would allow bug-fixes or enhancements to be installed in the network without PROM burning and mountain climbing. Painless software upgrading is essential if

[1]The board is designed to support 12 MHz 80186 chips. However, because the NEC DMA chips are not yet available in 10 or 12 MHz versions, initial boards will use 8 MHz processors.

[2]DMA stands for Direct Memory Access. It is a technique where sequential I/O operations are carried out by hardware in order to reduce processor load.

we want the networks to evolve. This requires that the switch contain a large amount of RAM, securely battery backed, and a secure mechanism for resetting the hardware remotely to initiate reload. (Amateur satellites have done this for years.) Some developers might not agree with this philosophy, so the board should contain massive amounts of ROM as well. We decided to design the board so that the processor's full 1 Mbyte address space could be populated with a variable mix of RAM and ROM. This required a design using 128Kx8 RAM chips that aren't quite available yet, so the design accommodates the use of smaller RAMs, with a corresponding temporary RAM limit of 256 Kbytes. We assume that prices of large static RAMs will continue to fall, but we added a bus expansion port capable of supporting an external RAM board just in case.

We questioned whether some applications might need more radio ports and if there should be a disk drive interface to support stand-alone development. Adding both the bus expansion port and a Small Computer System Interface (SCSI) port was the answer. The SCSI port can be used to interconnect several PS-186 boards, future expansion boards, a TAPR NNC (which also has a SCSI port), disk drives, etc.

Most existing TNCs generate significant RFI. A key issue was, therefore, to design a packet switch with RF-compatibility in mind. Because this board has more interfaces than most, there are many opportunities to introduce RFI problems, so we took special care. We decided that all digital circuitry should be above a complete ground plane — implying a multilayer circuit board.

As the feature list grew, affordability became a major consideration. We were afraid that we might be designing something so expensive that most hams couldn't afford one. Our solution was to make the board completely modular. This required considerable additional design time, and lots of option jumpers. Almost every chip on the board is now optional. Only users who require high-speed operation need install the DMA chips. Only users who require a SCSI port need install the SCSI chip. Ditto the real-time-clock chip, etc. Lower cost NMOS chips can be used in place of CMOS devices in most cases. Peripheral chips slower than the processor can optionally be used by running them on a ÷2 clock (with reduced performance of course), and on and on.

Finally, we hoped it would all fit on one board, and it did!

SOFTWARE CONSIDERATIONS

This switch is intended to serve as a hardware host for all the evolving packet radio protocols. We're not taking sides in the protocol wars. We expect that the developers of COSI, TEXNET, KA9Q's TCP/IP, and NET/ROM will all be able to port their software to the PS-186. As described in a companion paper, Brian Kantor, WB6CYT, is developing a multitasking operating system kernel for the PS-186, which may form the basis for future software developments.

WHAT WE BUILT

A specification summary of what evolved as the PS-186 follows. As you can see from this list, the PS-186 is designed to take advantage of many high-technology chips. Several other high-tech parts are not directly apparent. For example: power control for the battery-backed RAMs is simplified by the use of Dallas Semiconductor nonvolatile controllers, and PALs[3] are used extensively to replace what would otherwise be very complex random logic. Without PALs, the board would have been *twice as large.* The combination of advanced technology and planning for future developments, especially in the areas of faster chips and larger RAMs, should allow the PS-186 a long life.

Processor: Intel 80186 @ 8 MHz
- Option for 10 or 12 MHz CPU
- Option for CMOS 80C186 (same speeds)

PROM: 16K to 256K bytes
- 2764 thru 271024 byte-wide EPROMs supported
- 28 or 32 pin devices
- Optional wait states

RAM: 16K to 1023K bytes
- Up to eight of' 6264, 62256, or 621024 supported
- 28 or 32 pin devices
- Battery backup optional for each pair of RAMs
- No wait states

[3]PALs are Programmable Array Logic chips.

Serial Channels: 2 or 4 ports
- 1 or 2 Zilog 8530A or CMOS 85C30
- Simultaneous full-duplex DMA on all 4 ports
- Sync or Async, NRZ or NRZI or bi-phase
- 1X, 16X, or 32X clocks
- Hardware capable of over 1 Mbit/second on all channels
- All basic signals: TXD, RXD, RXclk, RTS, CTS, outbound TXclk, inbound TXclk, DTR, CD
- TTL voltage levels
- Small daughter boards per serial channel for level conversion or small modems

SCSI Port
- NCR 5380 or CMOS NCR 53C80 chip
- SCSI-Plus, initiator or target, ANSI X3T9.2 Compatible

Interrupt Controller
- Intel 8259A
- Wired for optional RMX-86 compatibility

DMA: 10 simultaneous DMA channels
- 2 channels inside 80186 -- used to support SCSI port
- 2 NEC 71071 chips provide 8 channels for serial ports

Time-of-Day Clock
- National DP857 1 chip
- Battery backed

Reset Circuits
- Power-on reset
- Manual reset
- Watchdog timeout reset
- Remote-reset circuit provides over-the-air reset

General Purpose I/O
- Bus expansion port w/DMA & interrupt support
- 4 bit option jumper
- 4 uncommitted LEDs

Power
- 5 Volt only operation
- 1.6 Amps using NMOS & ALS-TTL (i.e., 8 Watts)
- 420 mA using all CMOS parts (i.e., only 2.1 Watts!)
- 12 Volt optional distributed to daughter boards only

Board
- 7.75" x 11.5" (same size as two $5\frac{1}{4}$" disk drives)
- 6-layer construction (GND, VCC, 4 signal layers)

SOME OBVIOUS QUESTIONS

Q: Can all those ports *really go* that fast simultaneously? Won't they overrun? Can memory keep up?

A: DMA operations use 4.5 clock cycles on average. In an 8 MHz machine, that means there can be up to 1.8 million byte DMA accesses/second. All 4 serial ports running 1 Mbit/sec RX & TX at the same time generate only 1 million bytes/second and would therefore consume a maximum of 56% of the memory cycles. Running four *full-duplex* ports at 1 Mbit/sec is an extremely aggressive configuration, and you would seldom expect all 8 channels to be active simultaneously, but even when they are, about half of the memory cycles are still available for the processor.

Q: Is the 186 processor *really* capable of keeping up with greater than 1 Mbit/second *throughput?*

A: It depends on how carefully the software is written. DMA I/O relieves the processor of the burden of handling each character, so that the processor now need only respond to interrupts at the end of every received and transmitted packet, and perform the protocol processing required by each received packet. Consider a configuration with two 1 Mbit/sec full-duplex ports, such as described on page 1. Assume a packet size of 512 bytes, and both ports saturated with traffic. At 1 Mbit/sec, that's one packet arriving every 2 milliseconds. First we look at how many instructions the 186 can execute in that time. On average, the processor's speed is determined by memory access. A word access uses 4 clock cycles, and an instruction requires on the average about 2 word accesses. So in an 8 MHz system, the 186 runs at about 1 million instructions per second (MIPS). Processor speed is reduced to about 0.7 MIPS, because DMA activity in this example may require as many as 28% of the memory cycles. Finally, in 2 ms of running at 0.7 MIPS, the 186 can execute about 1400 instructions. That's enough for carefully written software to process the average packet and send it on its way. Note that packet size is an important parameter on high data rate links, because it determines the maximum packet arrival rate, and therefore processor throughput.

Q: Is it really necessary to build your own custom processor board in 1987? Why not use a personal computer or clone board?

A: Existing PCs and clones don't have the required I/O capacity. They aren't battery backed. They draw too much power. IBM PC system board clones, which are attractively priced, have only byte-wide memory, hence lack the processor speed or memory

cycles to support the I/O we have in mind. They do contain three DMA channels, but design constraints keep them from being used simultaneously. The IBM AT system board comes closer, but it still has some awkward DMA limitations, it would require the addition of a fairly complex. I/O board, it still wouldn't be battery backed, and would draw too much power for many applications. The MAC II has the same problems at a higher price. Personal computers weren't designed to be packet switches.

Q: Why no power supply on the board?

A: We didn't want to put a series-pass regulator for 12V operation on the board because it would dissipate over 14 Watts in the worst case (fully loaded NMOS). We didn't want to design in a switching power supply because we aren't power-supply engineers. Besides, this board is designed to be part of a system. There will be some modems also needing power. A single external power supply for the PS-186 and modems seemed a reasonable solution.

Q: Why TTL I/O? Why no RS-232?

A: Most of the modems we had in mind use or will use TTL I/O. Others may use V.35 or RS-422,. RS-232 interfaces are the exception rather than the rule at data rates above 19.2 kb/s. Each serial port provides a connector for a small daughter board which can con tain level translators, and appropriate connectors. A daughter board which converts a port to RS-232 has been designed for those applications requiring RS-232.

DETAILED CIRCUIT DESCRIPTIONS

The following describes the PS-186 hardware in considerable detail. Casual readers may wish to skip to the next section. It will be useful to refer to the block diagram and schematic. Reference designators refer to the schematic.

80186 Microprocessor

The Intel 80186 microprocessor at U12 provides the central core of the PS-186. This processor is capable of directly addressing up to 1 Mbyte of memory and 64 kbytes of I/O. The 80186 has many useful features (on-chip address decoding, wait-state generation, DMA controllers, and counters), and we use most of them. The on-chip memory and I/O decoding simplifies and reduces the logic. One of the two DMA channels is used to support an optional SCSI port and the timers are used for various software functions. Unused CPU features (one DMA channel, timer/counter inputs, etc.) are accessible at W16, W20, El, and E2.

The processor is buffered by chips U8, U9, U13, U14, and U27. This improves circuit loading characteristics, provides isolation, and demultiplexes the processor's address and data lines. U31 buffers the read and write lines and separates them into memory read, memory write, I/O read, and I/O write. The I/O write signal is delayed by flip-flop U30 to provide data setup time for peripherals.

Clock speed configuration jumpers W21 and W25 permit the use of various speed parts. The top frequency of the board (2x CPU clock) is established by hybrid oscillator Y 1.

EPROMs

Two byte-wide EPROM sockets are provided at U2 and U17. Each EPROM supplies one byte of a 16-bit word. Address configuration jumpers W2, W3, and W18 specify 16K x 8 chips (2764s) up to 128K x 8 chips (271024s). The maximum amount of EPROM is 256 kbytes.

The EPROMs reside at the very top of the CPU memory space, which is where the processor starts executing after it wakes up from a reset. Software configured EPROM sizing determines how far down in memory EPROM extends., This dynamic mapping of high memory allows, for example, programs to map in EPROM, read some data tables, and then map RAM back in. This scheme makes possible memory configurations greater than 1 Mbyte, even though the processor can only see 1 Mbyte at any time. The minimum software configurable EPROM is 1 kbyte.

The CPU, under program control, can insert up to three wait states allowing the use of almost any speed EPROM.

RAM

The PS-186 has space for up to four pairs of byte wide static RAMs (eight devices) at U3 & U18, U4 & U19, U5 & U20, U6 & U21. Three sizes of RAM chip can be used, 8K x 8 (6264), 32K x 8 (62256), or 128K x 8 (621024), selected by W5, W27, and W28. A board configured with eight 128K x 8 RAMs uses the full 1 Mbyte CPU address space, with some of the top-most locations lost to EPROM as previously I;";&--cussed.

RAM is optionally battery backed. Power for each pair of RAM chips is individually configured for Vcc

or a battery source by W4, W6, W7, and W8. The optional battery with all the switching and isolation required is included on the board. U36 provides the final section of RAM decoding and power isolation when a battery is used. A lower cost chip at U35 does this if battery backup is not required. The RAM isolation chip can switch up to 40 µA of backup power to the RAM. If the total RAM standby current exceeds this, an optional power control chip can be installed at U44 and enabled by jumper W33. W15 is used if there is no battery in the system. When deciding whether to include a battery, keep in mind that the time-of-day clock requires a battery if it is to continue timekeeping during power failures.

PAL U28 determines how much memory space the processor has allocated to EPROM and prevents the CPU from accessing RAM in that address range. It steers the memory write signal so byte writes don't disturb the other half of the word, and uses the RAM size configuration to determine which RAM pair to enable.

Serial Channels

Two Zilog 8530s at U54 and U55 provide four full duplex serial channels with modem control. The 8530s support synchronous and asynchronous serial line formats including support of bit and byte oriented synchronous protocols. These chips include baud rate generators as well as phase lock loop clock recovery circuits. Clock option jumpers allow the use of any speed 8530.

One of the unique features of the PS-186 is the 8530 control circuitry. This circuit takes care of the special timing requirements of the 8530s, eliminating the need for special programming, and allowing full use of DMA. The circuitry optimizes system performance by overlapping 8530 valid access recovery times and blocking DMA requests from individual 8530s while they are recovering. This maximizes the time available to the CPU. It also maximizes 8530 access since one 8530 can be serviced while the other is recovering. Recovery time is configured by W39, which specifies time constants for the two timing counters (U50 and U51). The counters are controlled by PAL U53 which performs timing optimization. The PAL also combines the read, write, and reset signals for the 8530s.

The 8530 interrupt acknowledge is synchronized by the flip-flops at U33. This allows full use of the 8530's interrupt vectors.

An extensive set of serial clock options is provided for each channel. W19, W22, W23, and W24 configure the outgoing transmit clock, incoming transmit clock, and incoming receive clock for channels A, B, C, and D, respectively. Provisions are made for 32x, 16x and lx clocks. Options specifically allow for a 32x or 16x baud rate clock from the 8530 to be divided down to lx externally and sent back to the 8530, making it possible to receive using the internal phase lock loop while maintaining a steady transmit rate.

The serial port connectors (J5, J6, J7, and J8 for channels A through D, respectively) are 16-pin header strips. All of the signals on these connectors are TTL. The board is layed out to accept small daughter boards which are large enough to contain an RS-232 interface, a TAPR modem disconnect interface, or even a full 1200 baud 202 modem. Filtered +5V and +12V power is supplied to each connector. Signals supported on the connector are: transmit data, receive data, RTS, CTS, DTR, DCD, incoming transmit clock, outgoing transmit clock, and incoming receive clock.

A byte multiplexer formed by U10, U15, and controlled by PAL U34, lets the 8530s respond to byte addresses. The multiplexer allows DMA operations with the 8530s to access sequential byte locations. The PAL also picks up some housekeeping functions to reduce part count.

DMA Channels

There are a total of IO *DMA channels* on the PS-186. Two of them are embedded in the processor. The first processor DMA channel supports the SCSI interface. The second is not associated with any device and may be used for memory-to-memory transfers.

The remaining eight DMA channels are provided by two NEC 7 1071 DMA chips and are dedicated to the serial channels. Two DMA channels are provided for each serial channel, resulting in full-duplex DMA operation. The DMA chips are capable of generating any RAM address without concern for address boundaries. The DMA chips do not see EPROM, and they always address RAM regardless of the processor memory map.

The DMA circuitry uses the fly-by mode of operation. This means that memory addresses are generated, I/O addresses are implied, and controls for both are activated simultaneously. During this operation the data is not stored anywhere, it just "flys by" on the bus, hence the name. Fly-by allows each byte DMA operation to complete in an average of 4.5 clock cycles. At 8 MHz,

this means over 1.7 million bytes/second, (i.e., over 14 Mbits/second) of DMA I/O are possible. Jumpers W9, W10, W11, W13, W30, and W31 permit either or both DMA chips to be removed.

Arbitration between DMA chips is provided by PAL U7. The PAL determines which controller will get the internal bus when a conflict. arises. It also arbitrates bus requests from the expansion port. Jumper W12 selects fixed or round-robin priority for the three requestors.

DMA chip interrupts are latched by U59 before being sent to the interrupt controller. These flip-flops are cleared by accessing specific I/O locations.

DMA interface to the 8530s is provided by PAL U52 and flip-flops U37 and U39. The PAL provides the implied I/O address required for fly-by DMA. The flip-flops provide a way to shut off the 8530 DMA requests once service has started, and an alternate way to start a transmit data stream. Accessing the I/O port associated with each flip-flop generates the first request to the DMA controller. This eliminates the need for the processor to send the first character of each DMA transfer directly to the 8530.

SCSI Port

To permit connection to other devices (TAPR NNCs, serial expansion boards, disk drives, or even other PS-186s) the PS-186 includes an optional NCR 5380 SCSI controller at U25. If the physically larger CMOS version of this chip is preferred it plugs in at U24. DMA channel 0 of the processor supports the SCSI port. The 220/330 ohm SCSI termination is provided by RN3 and RN4. W14 selects an internal or external power source for the termination. The internal power source is filtered and fused before it supplies any termination power, internal or external. The external SCSI connector, J3, is a standard 50-pin header.

Support for the SCSI chip is provided by the PIO (8255) at U43. Port A of the PIO is connected to 8 jumpers (W32) which set the SCSI address. The combination of an eight bit address and the 5380 chip permits use of the SCSI-Plus enhancements.

Interrupt Controller

Interrupts are handled by both the processor and an Intel 8259 at U40. The processor accepts interrupts and vectors from the 8530s, and by means of cascading, the 8259. The 8259 accepts interrupts from the DMA chips, SCSI chip, time-of-day clock, and bus expansion connector.

Time-of-Day Clock

A National DP8571 at U56 provides full clock calendar functions for the PS-186. The chip generates two distinct interrupts based on various alarm and timing functions. If a battery is supplied, the chip will continue timekeeping during power outages. Trim capacitor C61 adjusts the clock timebase.

PIO

An Intel 8255 PIO at U43 to provides a number of services to the board. PIO port A supplies the SCSI port address as discussed above. Port B is connected to W37, a four position jumper block set aside for software options. The other four bits of port B read the reset status of the board. By reading these, the software can determine the source of a hardware reset (power-on, manual, watchdog, remote). Port C is an output port divided into two halves. The first half drives the DTR lines on each serial port connector. The other half drives four independent LEDs which are used by the software to indicate program status or other conditions. W1 removes power from the LEDs when they are not in use,

Watchdog Timer

The reset control chip at U1 provides three services. The first is a watchdog function. If the watchdog I/O location is not accessed at least once every second, Ul generates a hardware reset. W40 enables or disables the watchdog. The second function is a reset switch debounce and sequencer. When switch Sl is pressed or contacts closed on de'bug connector J2, the board is reset and held that way for 250 ms after the switch is released. The third function is to hold the board in a reset condition when Vcc is out of tolerance and for 250 ms after the power stabilizes. This restrains the CPU during power transients

Remote Reset Circuit

This circuit provides a remote processor reset capability. The 4th radio port, channel D, is monitored for the presence of a 255 bit long pattern (PN^4 sequence). These patterns are long enough so that they will never occur accidentally in random data (an unsquelched rnodem input may produce continuous random data). They also contain sequences of l's which violate HDLC bit-stuffing rules, so that they cannot occur in valid HDLC frames.

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[4] PN sequences are also sometimes called "maximal-length-shift-register-sequences". They are patterns of l's and O's that are easy to generate, and have nice statistical properties.

During normal operation, the *8530* SCC chips do bit synchronization for incoming data. Unfortunately, the reset circuit must operate assuming the processor has crashed, so cannot make use of the 8530s. PAL U48 is an optional bit-timing recovery state-machine. Jumper W35 selects NRZ or NRZI output, or bypasses U48 entirely for those modems that do their own bit-synchronization. Jumper W34 selects between the recovered clock or an optional clock from the modem. PAL U46 searches the input data stream for the reset sequence.

The PAL has been programmed to search for one of 12 PN sequences[5] selected by jumper W38. We didn't want a reset command to accidentally trigger every PS-186 within hearing range of the sender. Our intention is that nearby PS-186 nodes will use different reset sequences, keeping them individually resettable.

When the reset sequence is detected, the circuit causes a non-maskable interrupt (also optional per jumper W29). This circuit interacts with the watchdog to initiate a timeout. If the software does not respond to the interrupt within a second, a hard processor reset is forced. The need for a remote hard reset is clear. For those who may want to implement a more sophisticated soft reset in software, this circuit provides that capability without sacrificing the hard reset needed when the processor is severely crashed.

Board Power

Power is supplied to the board through a standard 4-pin disk drive style connector at J1. The board is expected to survive in noisy environments so attention was given to filtering and bypassing. As power enters the board it is filtered by ferrite beads and capacitors. At each individual serial port connector the power is again filtered and bypassed by ferrite beads and capacitors. The liberal use of bypass capacitors and a multilayer circuit board with power planes keep the noise and susceptibility down.

Both +5 and +12 Volts are brought in from the power connector but only +5V is used on the board. The +12V is supplied to the serial port connectors in case the daughter boards require it.

Bus Expansion Port

A 60-pin bus expansion connector, J4, provides expandability. J4 contains all the address, data, and control lines necessary to add external peripheral devices, bus request and acknowledge lines to support external DMA chips, two interrupt lines, and of course, power.

SCHEDULE & AVAILABILITY

The project began in a meeting between KB5MU, KA6IQA, WB6HHV in May of 1985, where the basic goals of the project were established. Design began in earnest a year later. A wirewrap prototype (see photo) was completed in July 1986, test code was running on the board in August, and the design was committed to printed circuit layout in November. PC layout was completed in July 1987. At times it seemed our progress gave new meaning to "slow". In retrospect, the only slow parts were "getting started" (an age-old schedule killer) and the board layout. We don't fault the people who donated their efforts for the 6-layer board layout. Charity work is necessarily low priority, so free services don't often fit any particular schedule.

The present schedule calls for ten assembled and tested development prototypes to be available in October. We feel lucky to have obtained donations from various manufacturers of most of the sophisticated integrated circuits required for the prototype build. We had to pay for boards, sockets, and many of the 'ordinary' ICs These protos will be made available to a (nedessarily limited) number of software developers who have demonstrated a capability to produce useful software products to the amateur radio community. The boards will come with test code and a debugger in EPROM, source on $5\frac{1}{4}$" IBM PC diskette, and a technical manual. We *hope* to make 2nd round production quantity boards available in January 1988. The distribution mechanism for production boards has not been worked out.

While we can make no guarantees about prices which may be offered by an eventual distributor, we hope bare boards will be made available for under $75. All parts on the PS-186 can be purchased in small quantities for $135. (for a minimum configuration) or $300. (maximum) from suppliers advertising in Byte magazine.

'There are 16 PN sequences of length 255, but we ran out of product terms in the PAL, so it only searches for 12 of them.

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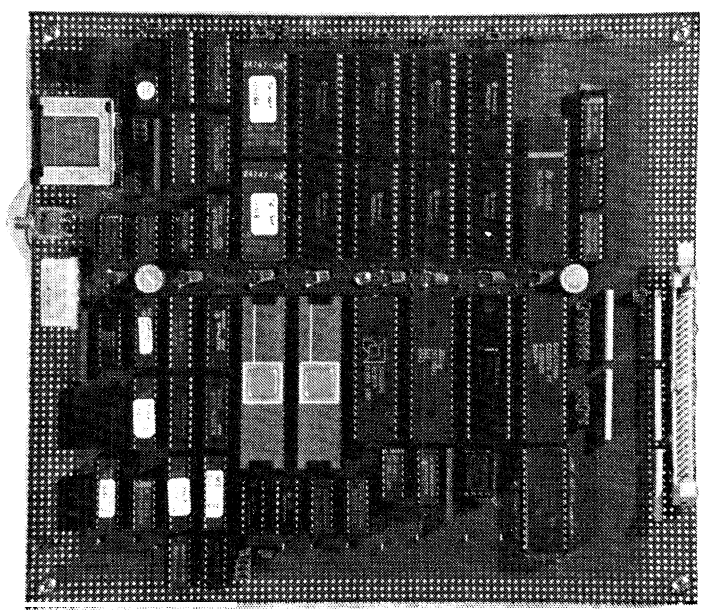
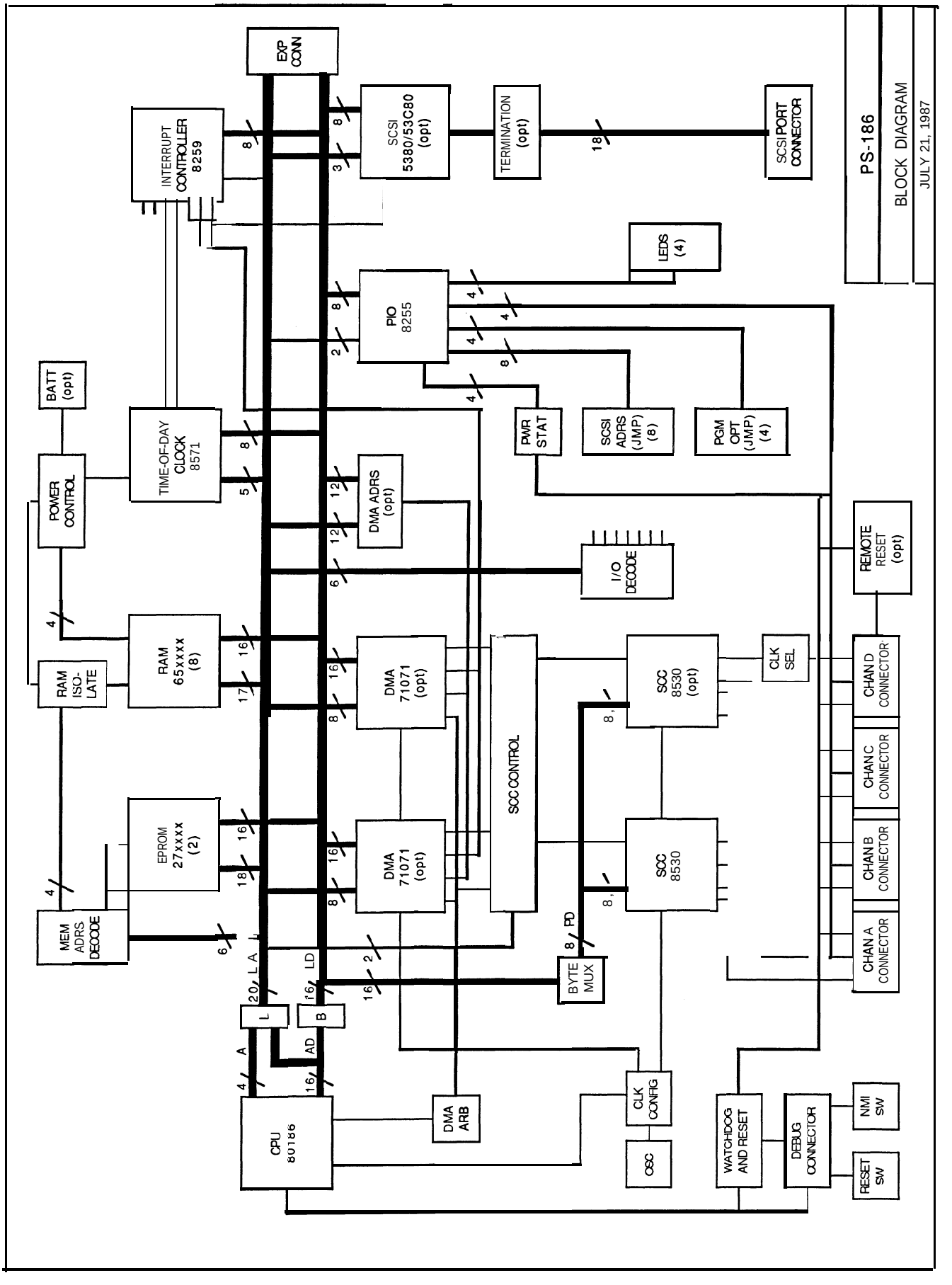
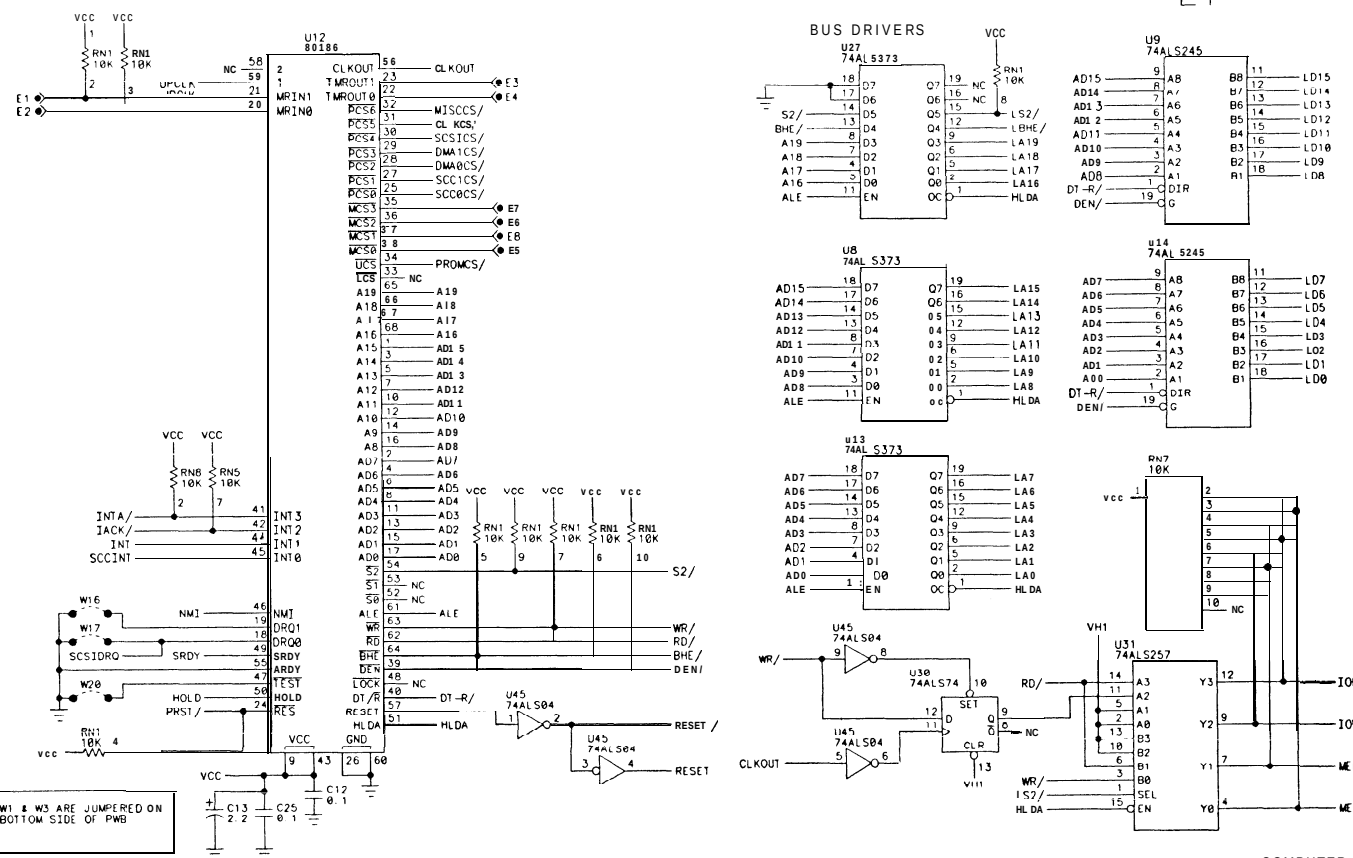


PS-186 Wirewrap Prototype


PS-186
BLOCK DIAGRAM
JULY 21, 1987
EXP CONN
INTERRUPT CONTROLLER 8259
SCSI 5380/53C80 (opt)
TERMINATION (opt)
SCSI PORT CONNECTOR
LEDS (4)
PIO 8255
BATT (opt)
TIME-OF-DAY CLOCK 8571
PWR STAT
SCSI ADRS (JMP) (8)
PGM OPT (JMP) (4)
POWER CONTROL
DMA ADRS (opt)
I/O DECODE
REMOTE RESET (opt)
RAM ISO-LATE
RAM 65xxxx (8)
DMA 71071 (opt)
SCC CONTROL
SCC 8530 (opt)
CLK SEL
CHAN D CONNECTOR
CHAN C CONNECTOR
EPROM 27xxxx (2)
DMA 71071 (opt)
SCC 8530
CHAN B CONNECTOR
MEM ADRS DECODE
BYTE MUX
CHAN A CONNECTOR
CPU 80186
DMA ARB
CLK CONFIG
OSC
WATCHDOG AND RESET
DEBUG CONNECTOR
NMI SW
RESET SW



5 INDUCTOR VALUES ARE IN MICROHENRIES

4 CAPACITOR VALUES ARE IN MICROFARADS

3 RESISTORS ARE IN OHMS. ±5%, 1/4 WATT

2 PART NUMBERS ARE ABBREVIATED AND FOR REFERENCE ONLY FOR COMPLETE PART NUMBERS, SEE PARTS LIST

1 INTERPRET DRAWING PER DOD-ST D-100

NOTES UNLESS OTHERWISE SPECIFIED

6 REFERENCE DOCUMENTS

ASSY DWG

PARTS LIST

REVISIONS			
RCV	DESCRIPTION	DATE	APPROVED
	RELEASE SEE DCR	-	-

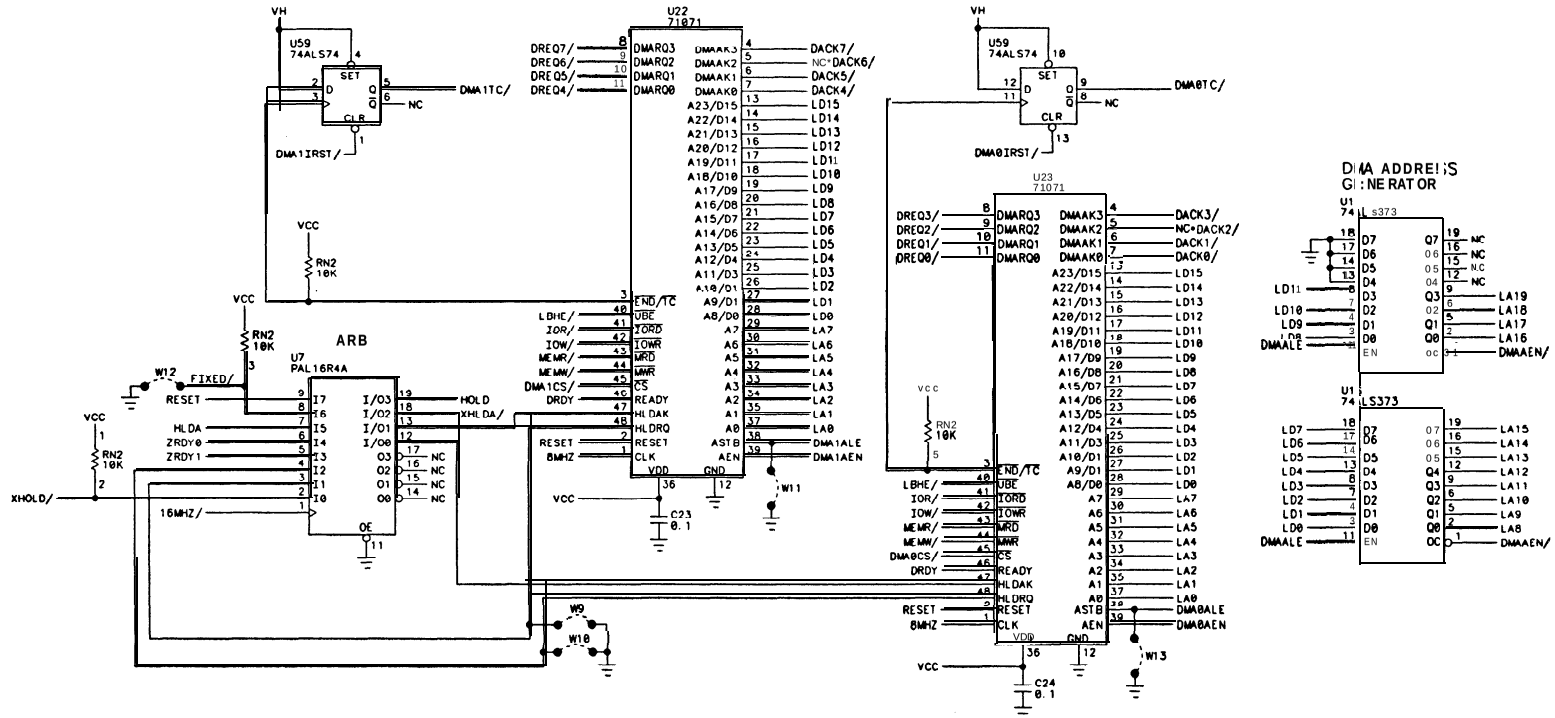
COMPUTER GENERATED DRAWING

	CONTRACT No	DATE	
	DRAWN		TITLE
	CHK		SCHEMAT J-C
	ENG		PS-1 86
	PROJ ENG		
	MFG		
	PTS CONT		
	LOG		SIZE B / CAGE NO / DRAWING NO LAFLEUR / REV
NEXT ASSY / USED ON	P A		
APPLICATION	RLSE		SCALE NONE / SHEET 1 OF

DWG NO	LAFLEUR	SHT 2

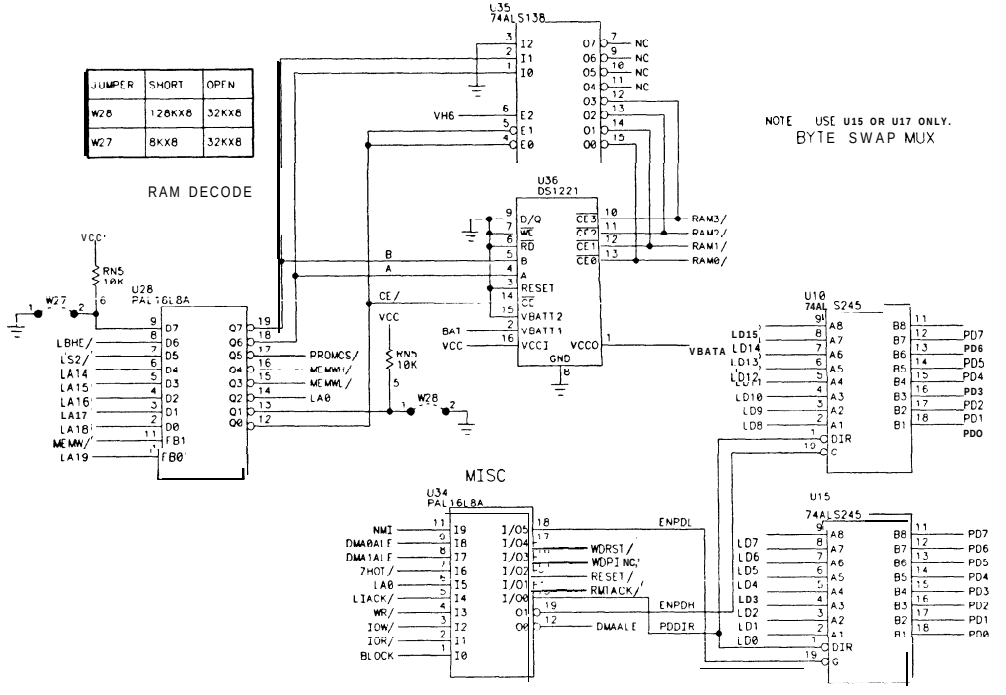
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
–	SEE SHEET 1		



DMA

PS-186	SIZE B	CAGE NO	DRAWING NO LAFLEUR	REV –
	SCALE: NONE		SHEET 2	



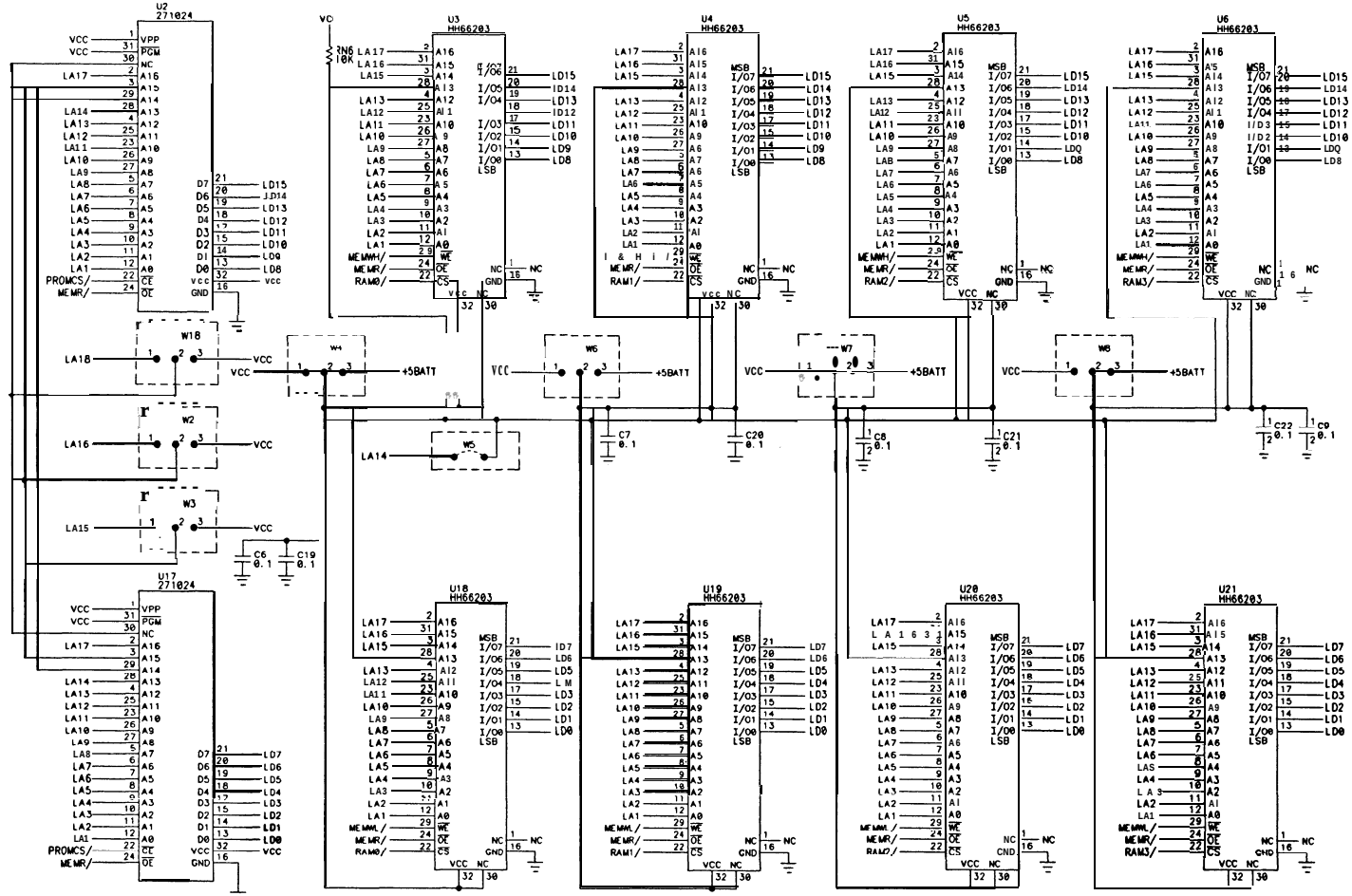
RAM DECODE
AND BYTE MUX

PS-186	SIZE B	CAGE NO	DRAWING NO LAFLEUR	REV -
	SCALE NONE		SHEET 3	

DWG NO	LAFLEUR	SHT 4

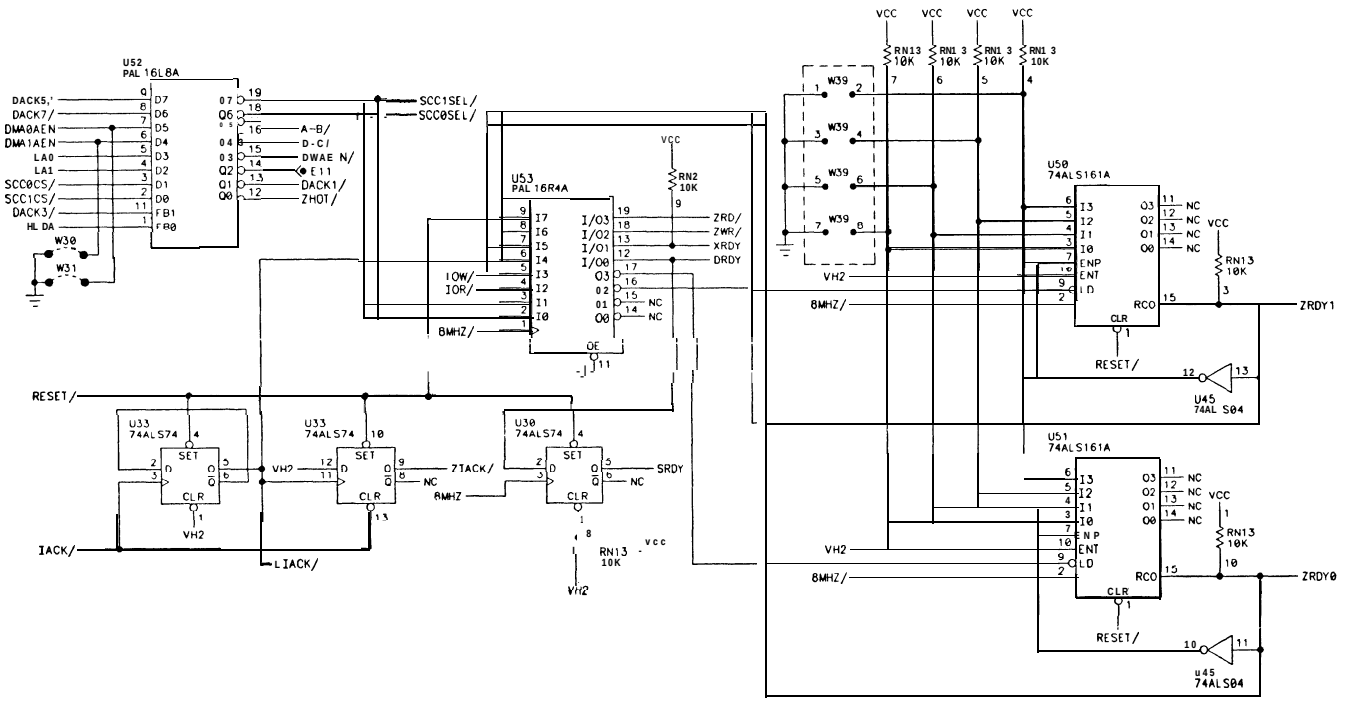
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
-	SEE SHEET 1	-	-



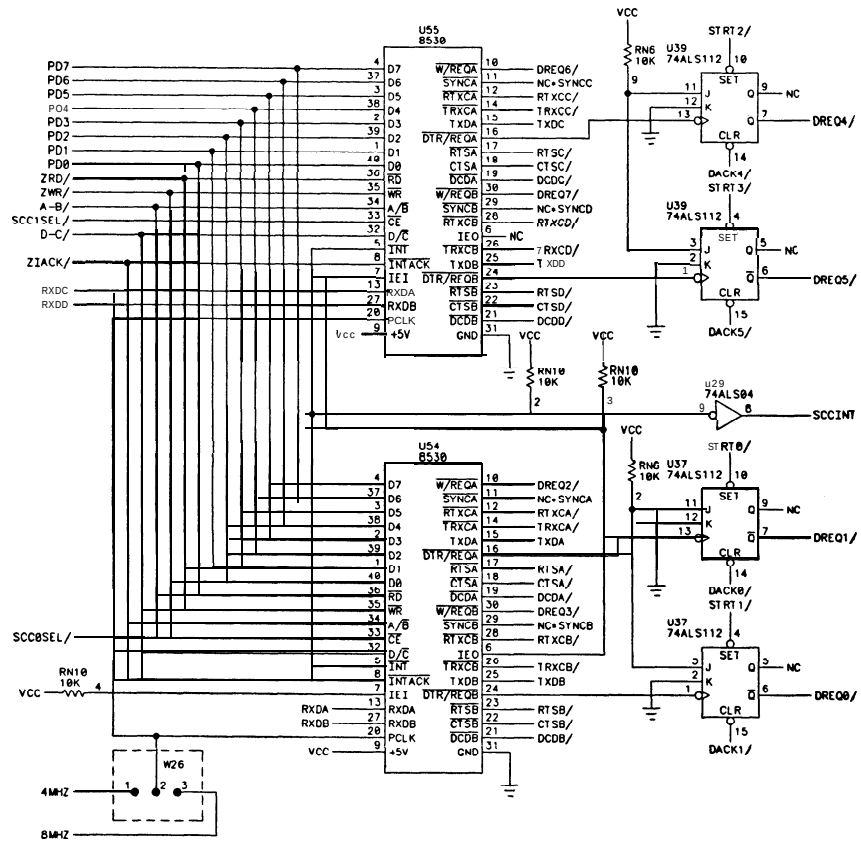
MEMORY ARRAY

PS-186	SIZE B	CAGE No	DRAWING NO LAFLEUR	REV -
	SCALE: NONE		SHEET 4	



SCC T IMING

Ps-186	SIZE B	CAGE NO	DRAWING NO LAFLEUR	REV -
	SCALE NONE		SHEET 5	



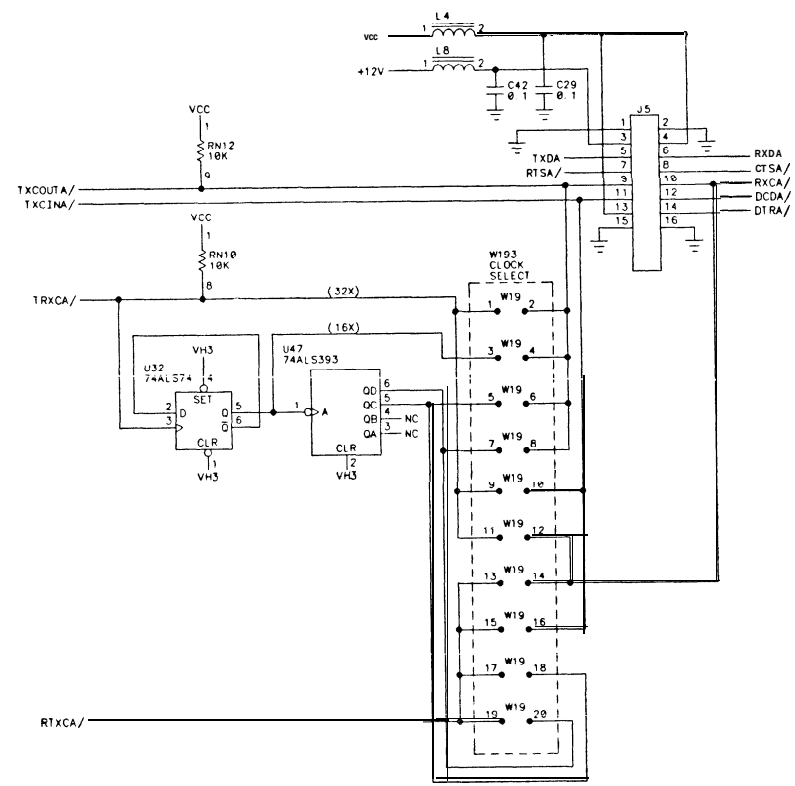
SCC

PS-186	SIZE B	CAGE No	DRAWING No LAFLEUR	REV –
	SCALE NONE		SHEET 6	

DWG NO LAFLEUR SHT 6

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
–	SEE SHEET 1	–	–



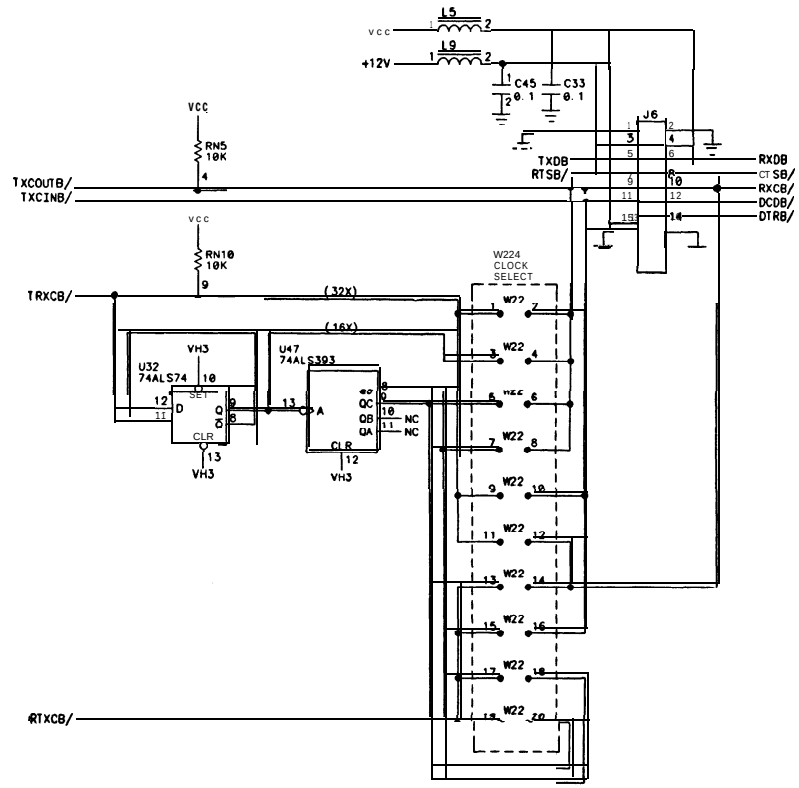
DTE CHANNEL A

PS-186	SIZE B	CAGE NO	DRAWING NO LAFLEUR	REV –
	SCALE NONE		SHEET 7	

DWG NO	SHT
LAFLEUR	8

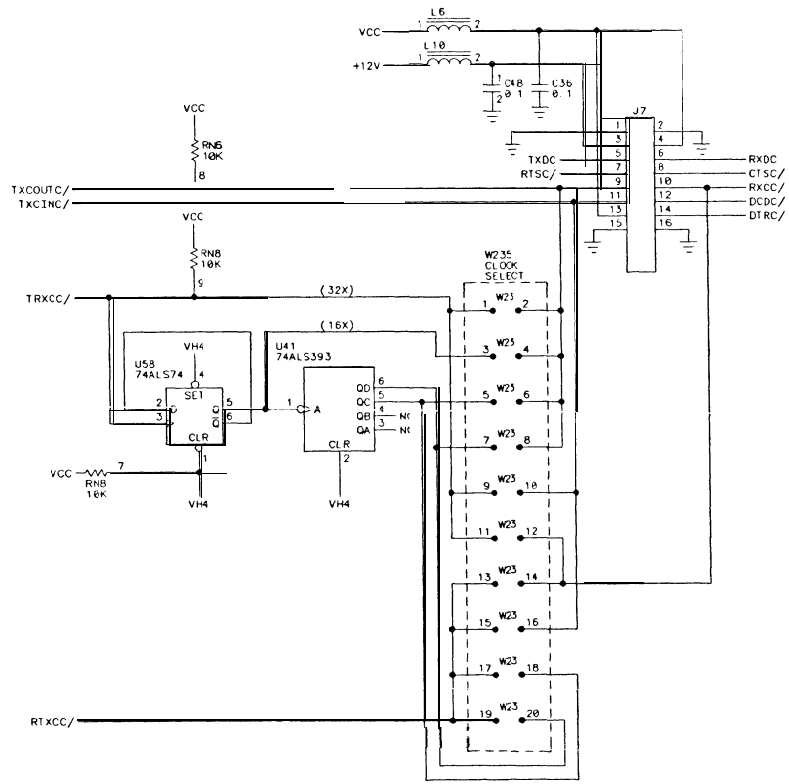
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
-	SEE SHEET 1		



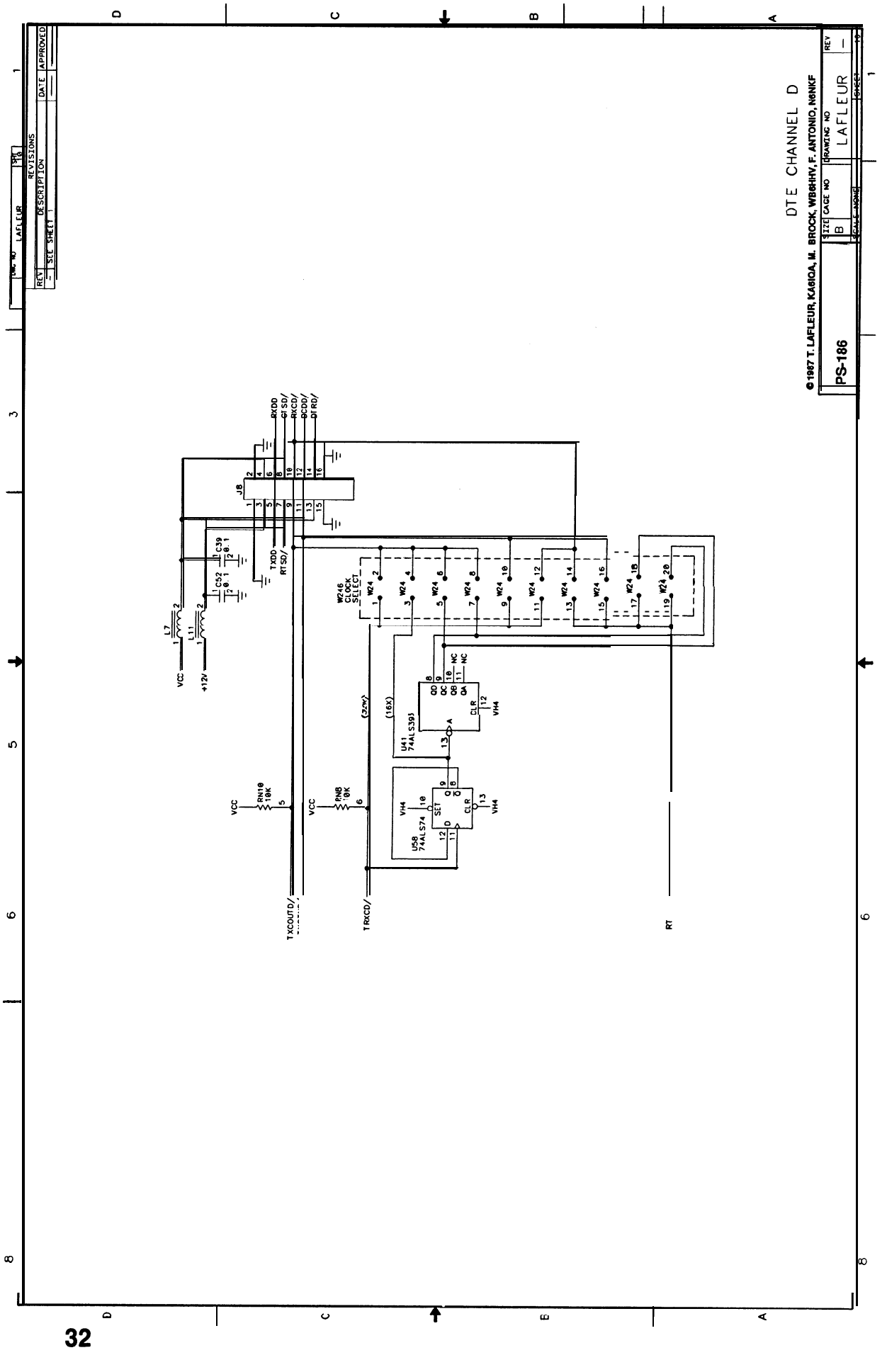
DTE CHANNEL B

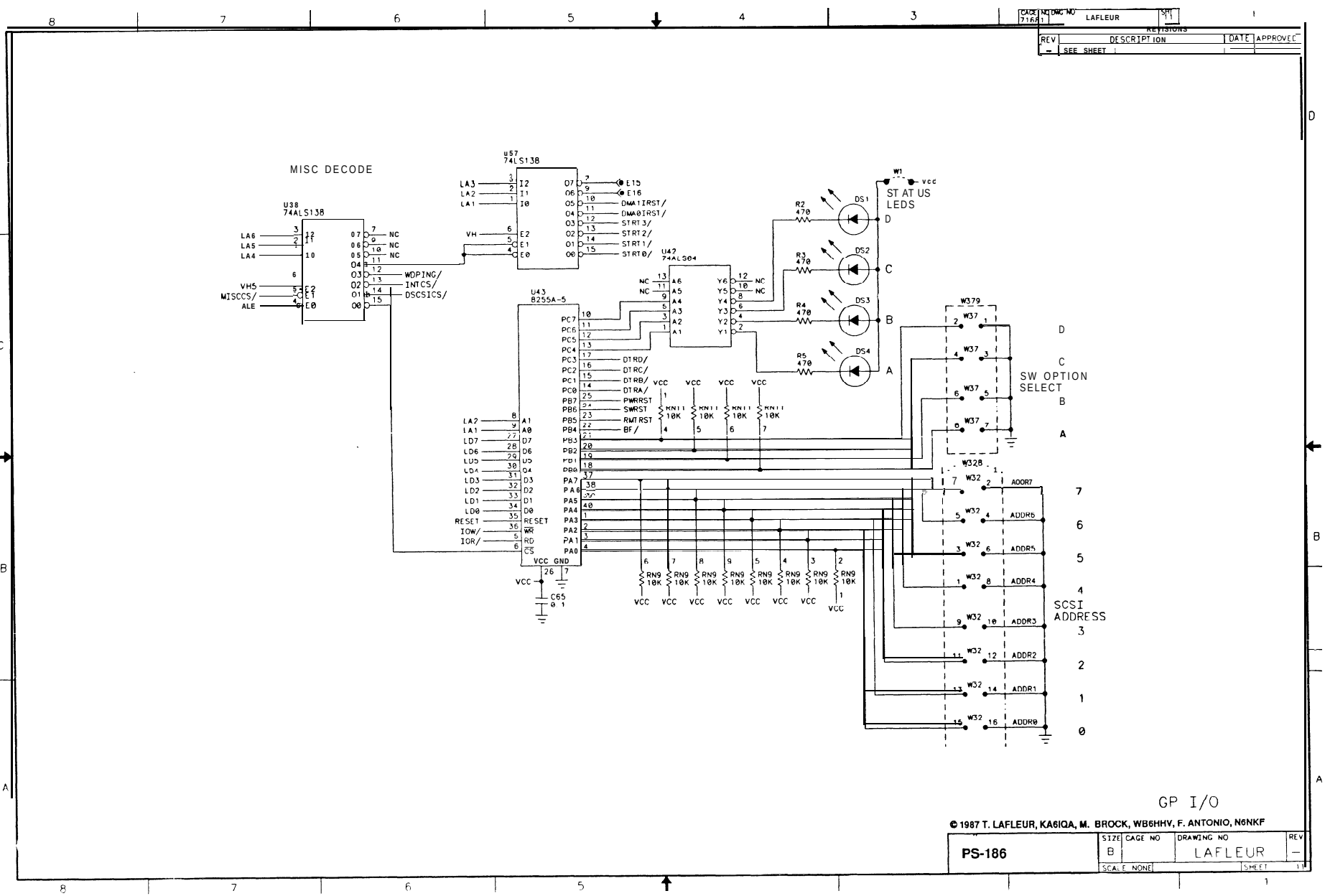
	SIZE	CAGE NO	DRAWING NO	REV
PS-186	B		LAFLEUR	-
	SCALE: NONE		SHEET	8

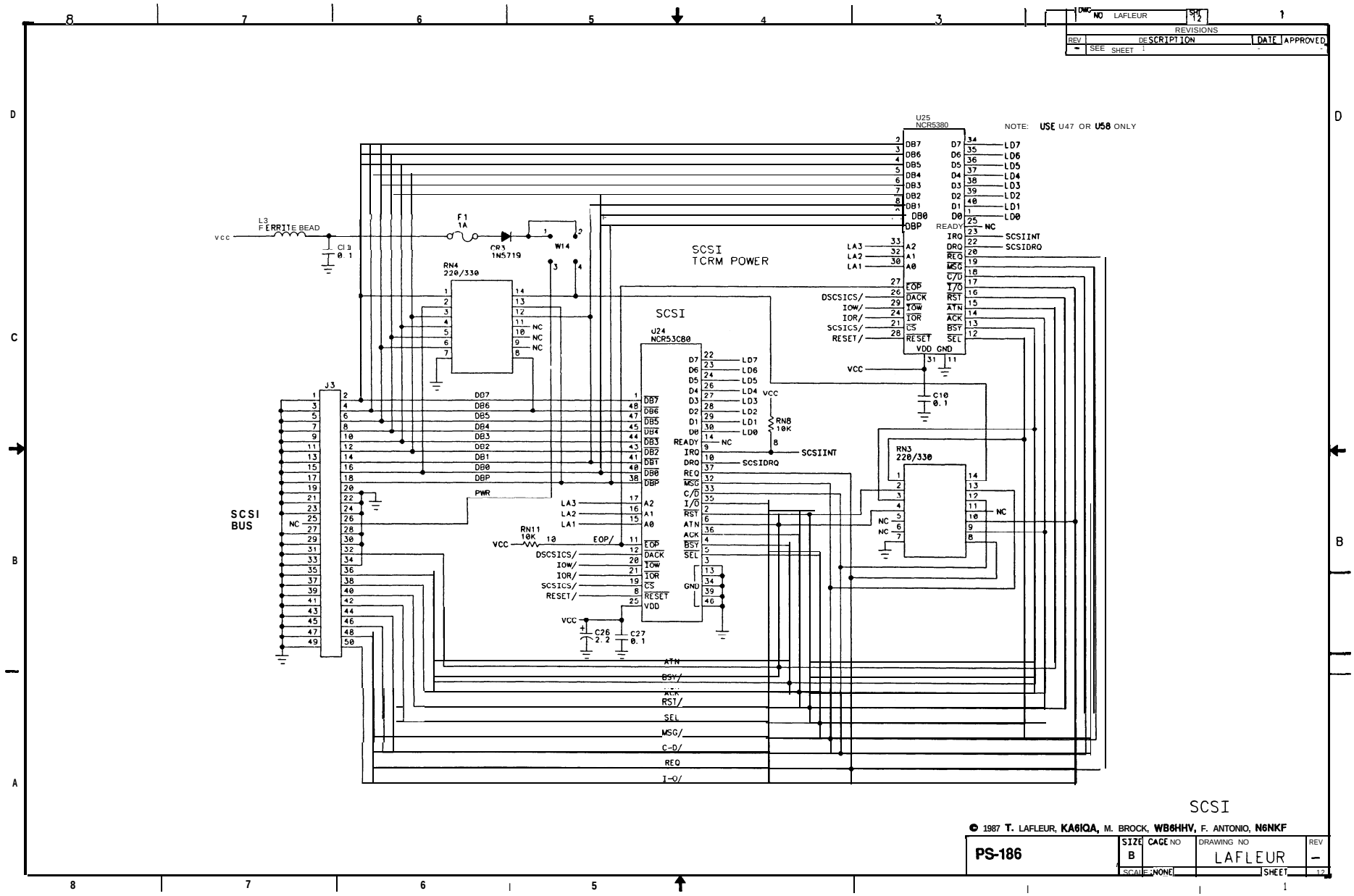


DTE CHANNEL C

PS-186	SIZE B	CAGE NO	DRAWING NO LAFLEUR	REV –
	SCALE NONE		SHEET 9	


DTE CHANNEL D
PS-186
LAFLEUR
© 1987 T. LAFLEUR, KA9IOA, M. BROCK, WB8HHV, F. ANTONIO, N6NKF
REVISIONS
DESCRIPTION
DATE
APPROVED
SEE SHEET 1
J8
RXDD
CTSD/
RXCD/
DCDD/
DTRD/
TXDD
RTSD/
C39
C52
L7
L11
VCC
+12V
W216
CLOCK
SELECT
W24
U41
74ALS393
(32X)
(16X)
QD
QC
QB
QA
CLR
NC
VH4
RN10
10K
RN8
U58
74ALS74
SET
TXCOUTD/
TRXCD/
RT

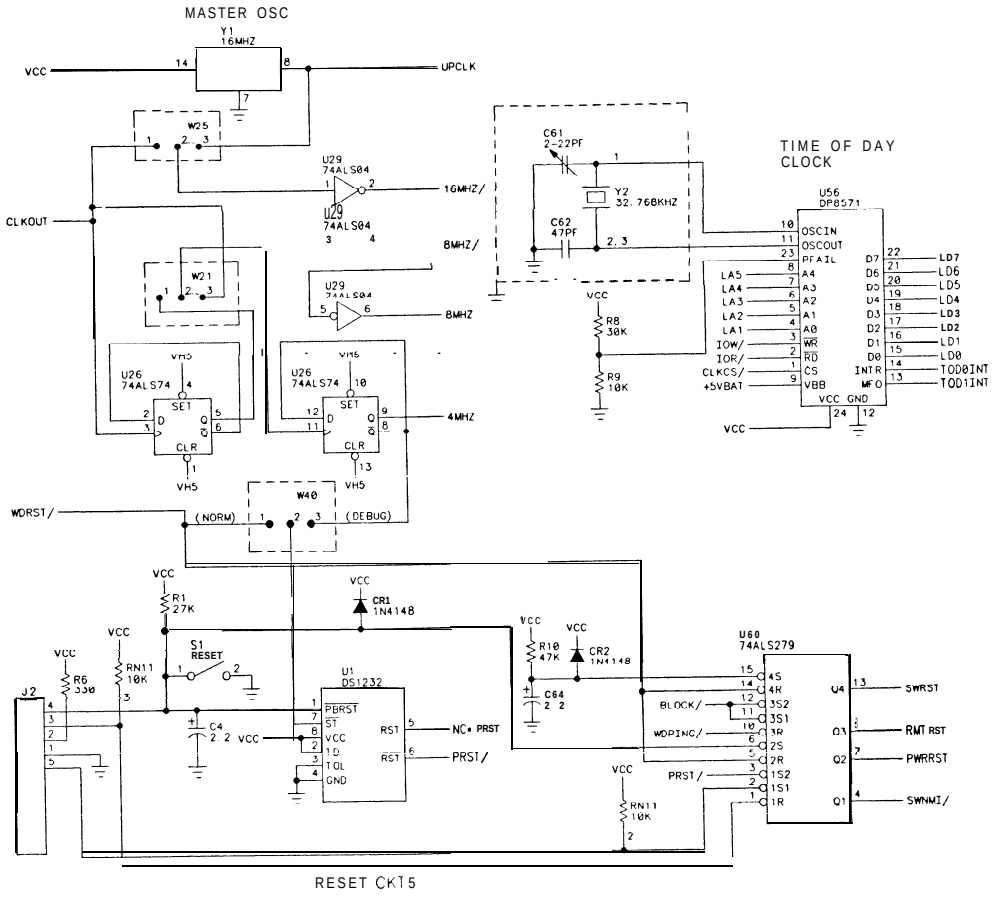

MISC DECODE
U38
74ALS138
U57
74LS138
U42
74ALS04
U43
8255A-5
W1
VCC
ST AT US
LEDS
DS1
DS2
DS3
DS4
R2 470
R3 470
R4 470
R5 470
D
C
B
A
W379
W37
SW OPTION
SELECT
W328
W32
SCSI
ADDRESS
7
6
5
4
3
2
1
0
ADDR7
ADDR6
ADDR5
ADDR4
ADDR3
ADDR2
ADDR1
ADDR0
LA6
LA5
LA4
VH5
MISCCS/
ALE
LA3
LA2
LA1
VH
WDPING/
INTCS/
OSCSICS/
DMA1IRST/
DMA0IRST/
STRT3/
STRT2/
STRT1/
STRT0/
E15
E16
DTRD/
DTRC/
DTRB/
DTRA/
PWRRST
SWRST
RWTRST
BF/
LA2
LA1
LD7
LD6
LD5
LD4
LD3
LD2
LD1
LD0
RESET
IOW/
IOR/
VCC GND
C65
0.1
KN11
10K
RN9
10K
GP I/O
© 1987 T. LAFLEUR, KA6IQA, M. BROCK, WB6HHV, F. ANTONIO, N6NKF
PS-186
SIZE B
CAGE NO
DRAWING NO LAFLEUR
REV –
SCALE NONE
SHEET 1/1
REVISIONS
REV DESCRIPTION DATE APPROVED
– SEE SHEET 1



PS-186

SCSI

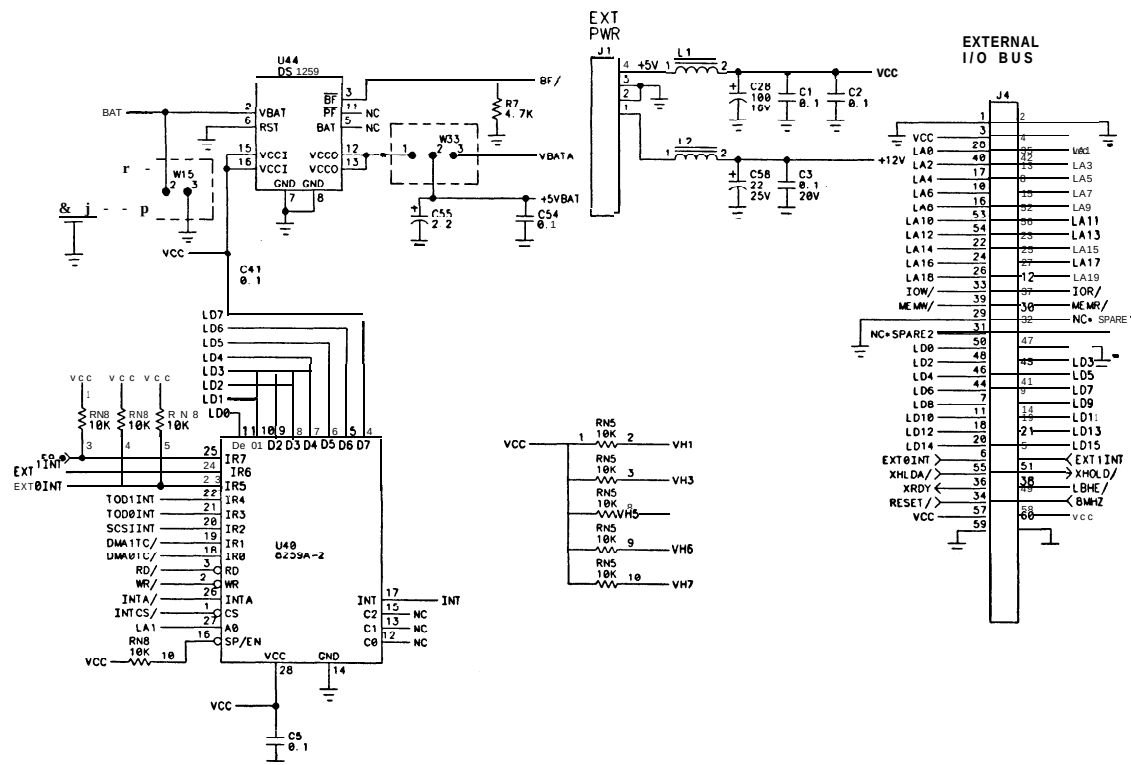
LAFLEUR



CLOCK AND RESET

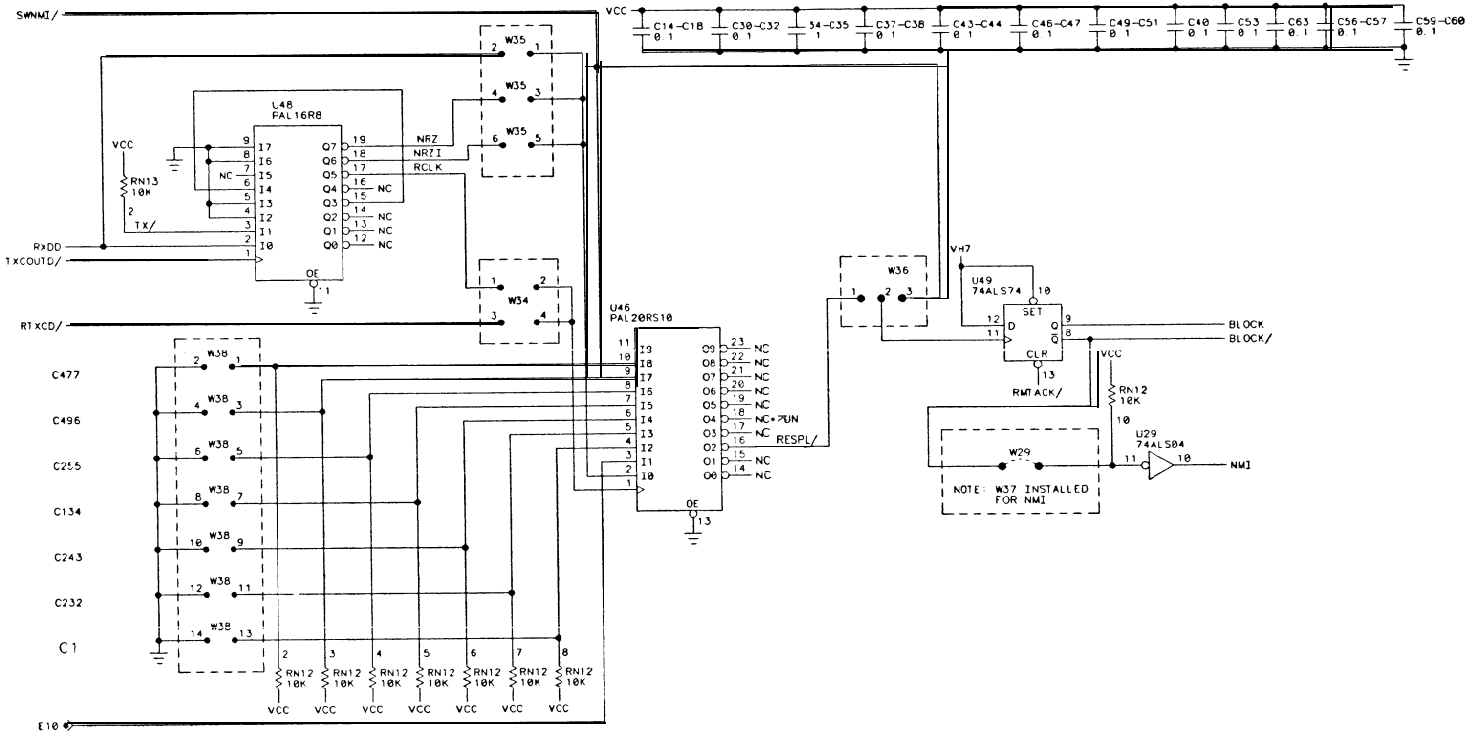
PS-186

SIZE B | CAGE NO | DRAWING NO LAFLEUR | REV 1
SCALE NONE | SHEET 13



INTERRUPTS AND EXT I/O

PS-186	SIZE B	CAGE No	DRAWING NO LAFLEUR	REV -
	SCALE NONE		SHEET 14	



REMOTE RESET

PS-186