A GPS DATA RECEIVER

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This paper describes the construction of a Global Positioning System (GPS) single channel data receiver using the **L1** carrier. A brief explanation of the GPS system is provided. The needed details of the GPS signal structure are also covered.

GPS uses Spread Spectrum techniques. It is one of the first world wide systems to implement this technology. These techniques will play an ever larger part in tomorrows communication systems.

The Global Positioning System

GPS is a satellite system that can provide users with time and position information. The satellites transmit satellite position and GPS time information to receivers on the ground or in the air. Orbits are half synchronous. There will be 18 satellites in the completed system. Nine satellites are up with the remainder to be installed within two years(?). Three satellites must be in view to obtain latitude and longitude (if altitude known). **Four** must be in view to obtain latitude, longitude and altitude. These two scenarios assume that the user receiver does not know GPS time. If position is known then GPS time can be obtained. When the system is complete this information will be available globally, twenty four hours a day.

GPS Signal Structure

The GPS signal uses two carriers **L1** and **L2**. **L1** is at 1575.42 MHz. L2 is at 1227.6 MHz. Both carriers have data information on them. All satellites use the same two frequencies. How does the user receiver know which satellite it is looking at? By use of a code that is impressed on both carriers that is unique to that satellite. Two codes are used: the C/A code and the P code. **L1** has both the C/A and the P code impressed on it. L2 has either the P or the C/A code impressed on it. The C/A code is a 1023 pseudo random binary sequence. This code is open to public usage and is not **"classified".** The P code is an extremely long pseudo random binary sequence that is not open to the public and is **"classified".** For this reason the L2 signal is ignored. This paper addresses only the particulars of **a L1** receiver. But the **L1** signal has the P code on it too so how can you receive **L1** with out knowing the P code? . It turns out that the method used for impressing the code(s)+data onto the carrier **L1** allows for this provision.

Figure one is a simplified model of the satellite **L1** generator. First note that all frequencies used are multiples of the 10.23 MHz reference. This is important and will be used later. We see from this diagram that the C/A code is at a 1.023 MHz rate while the P code is at a 10.23 MHz rate. The data clock is 50 Hz. It is derived from detecting the all ones state (10 **1's** in a row) of the C/A code, this occurs once every 1023 bits so this is at a 1 **kHz** frequency, and

dividing by 20. The two codes are exclusive OR'ed with the data to form the two BPSK modulating sources. The summation of these components results in a QPSK signal. Because of the 90 degree phase difference and the carrier spreading caused by the P code it is possible to build a C/A code BPSK receiver. In other words the P + DATA modulation on L1 can be ignored. That is what the receiver addressed in this paper does.

The minimum received power at the earths surface is -130 dBm for a 0 dB gain antenna. The satellite sends this out RH circular polarized. Due to the spreading of the C/A code the L1 signal is below the noise floor of the receiver. It can only be seen if the receiver has a copy of the C/A code to raise it "out of the mud" of the receiver noise. This process is called correlation and is at the heart of GPS receivers.

Figure 3 shows the spectrum of the L1 signal. The spectrum shows how the P code sin(x)/x envelope is below that of the C/A code sin(x)/x envelope.

The C/A Code

The C/A code modulation is far and away the most complicating aspect of this receiver. But without it the system would not work. So what does the C/A code do for us? First and foremost it allows **"multiple access,"** or simply the ability for all the satellites to use the same frequency(s) to send data on. Without it a receiver would see a jumble of signals from all satellites in view. Anti-jam. The C/A code will reduce a offending CW signal that finds its way into the receiver by approximately 35 dB. The C/A code allows accurate determination of the distance between the satellites and the receiver. And as previously mentioned retrieves the L1 signal from below the noise floor. So although it may seem the C/A code adds needless complication it is vital to the operation of GPS receivers.

As noted above the C/A code repeats every 1023 bits. This repetition marker decoded from the all 1's state is called a epoch. The C/A code can be generated by two ten stage shift registers with appropriate tap points. Figure two shows the two shift register and the interconnections needed. The tap points on register G2 determine a unique C/A code for each satellite. Table 1 is a list of the tap points used for each satellite. Whenever a carrier is modulated by codes such as the C/A code this is referred to as "spreading" due to the resulting increase in bandwidth. The receivers job is to remove the C/A code (despread) so as to retrieve the data modulation. When a receiver has its code lined up with a satellites code and keeps it this way it is said to have code lock. When in code lock the receivers C/A code epochs are in sync with the transmitted C/A code epochs. A very important detail regarding the C/A code and for that matter the entire GPS system is that all satellites are synchronous. In other words the C/A code epochs are all lined up for all satellites at transmission time. This fact is used to make the position measurement.

Doppler

The velocity difference between the satellite and the user receiver causes a Doppler shift of the L1 carrier. This is on the

order of +7.0 **kHz** to -7.0 **kHz.** This causes some problems for the receiver. The problem stems from the low signal level of the received **L1** signal. This forces a narrow IF bandwidth of approximately **1 kHz** to achieve a tolerable SNR. To over come the Doppler the receiver must scan the possible Dopplers and then once the signal falls inside the 1 **kHz** IF filter it must keep it there using some sort of Doppler tracker. The Doppler is also present on the C/A code clock of 1.023 MHz. This is due to the coherent nature of the transmitter. The Doppler on the code clock is equal to the Doppler on the carrier divided **by** 1540, the multiplying factor between the 1575.42 MHz carrier and the code clock at 1.023 **MHz.** So for 7 **kHz** Doppler on the carrier we see approximately a 7 Hz Doppler on the code clock. Again the receiver must be able to tolerate this offset.

Data Modulation/Demodulation

Figure 1 shows that the GPS data rate is 50 bits per second. Ignoring the code modulation for the moment the data stream modulates the carrier via the BPSK modulator. Being that the content of the data stream is fairly complex, discussion of this will be postponed for now, Once the receiver removes the C/A code and has Doppler lock data demodulation can take place. Any type of BPSK demodulator can be used. I used one based on a PLL but many of the designs in the literature use the **Costas** loop demodulator.

Position Measurement

Although the receiver described in this paper does not make the position measurement some words on this are needed.

The key to the position measurement is the fact that all satellites are synchronous. This means that **at** all of the satellite transmitters the C/A code epochs are **"lined up".** This is indicated in figure 4. But to the user the epochs arrive at different times due to the different path lengths. Again see figure 4. These differences in path lengths are called pseudo ranges. It is the receivers job to measure these time of arrival differences **w.r.t.** his own clock and then compute the pseudo ranges and solve for user position and clock bias **w.r.t.** GPS time. This involves solving a system of four equations with four unknowns given the pseudo ranges and satellite positions from the measurements and satellite data. The equations are shown in figure 4.

The measurement of the path delays or pseudo ranges presents a problem for the single channel receiver such as the one described here. The single channel receiver must acquire and track four satellites sequentially as opposed to a four channel receiver which can track four satellites simultaneously.

If the user knows any one of the four unknowns an equation can be eliminated. The complexity of the sequential tracking and the solution of the equations requires a computer interface and **a** companion program. Also needed is a high speed digital latch to measure the path delays. At this time I have not pursued the position problem.

First Things First

Before anything can happen in the receiver whether its Doppler tracking, data demodulation or position measurement the receiver must line up its own generated C/A code with that of the transmitted **L1** signal. If the two codes are not within two **"chips"** of alignment there is no signal for Doppler, data etc. A **"chip"** is the duration or length of one bit of code. This **was** for me the toughest problem to solve primarily because this is the one aspect of a GPS receiver that is completely different from conventional receivers. The method used to obtain code lock is the **Tau-Dither** circuit. This is a well documented method **(but** no actual circuits!) and is found in the references provided. I will leave the details of my implementation of this technique for later when the receiver hardware is discussed.

Why Build a GPS Data Only Receiver?

There are right now many commercially made GPS receivers on the market. I wanted to build my own receiver to 1) educate myself on receiver design, this is my first 2) Build a receiver that others could understand and if not duplicate have a good starting point 3) Be able to write this article that I hope will fill the void that currently exists in the literature on GPS and spread spectrum systems in general; a complete detailed description of an entire receiver. A benefit of this design is the fact that it is nearly all analog. Many of the commercial receivers digitize the IF and the signal disappears into a black box of digital signal processing. This is great from a cost/performance point of view but not from a intuition and learning point of view. The analog approach lends itself more to seeing the various and different trade offs in the design especially in the code tracking loop. And although the position problem is not addressed getting the data in **my** opinion is the toughest nut and has the most **"fruits"** to be gained. The data only receiver gives excellent insights that can be applied to other spread spectrum systems.

A L1 Data Receiver

Figure 5 shows a block diagram of the receiver. Some representative spectrums are shown at various points. The **L1** signal is received using a quadrafilar circularly polarize antenna. The signal then enters a LNA. From here the signal goes through 60 feet of **RG-214** (RG-213 could be used) to the crystal down converter. The down converter converts the spectrum at 1575.42 MHz to the 1st IF of 28.644 MHz. After passing through the 1st IF amp the signal comes to the **Mixer/Correlator.** This is just a DBM used in a slightly different way to achieve the 2nd IF of 5.7288 MHz. The only difference from conventional **down** conversion here is that the 2nd LO is phase modulated **by** the receivers own C/A code generator. This is where the C/A code is removed. If the receiver generated code is lined up with the code from the satellite then the 2nd IF will be present otherwise the receiver sees only noise. Assuming the codes are locked the 2nd IF spectrum is as shown. All the **LO's** for the **2nd,** 3rd and 4th **IFs** are generated by division of the 114.613 MHz VCXO. The **VCXO** is needed here to compensate for Doppler and is controlled by the Doppler Scan/Track

circuitry. From the 2nd IF the signal goes through two more **IF's** to the final IF of 20 **kHz.** This low IF is chosen so that active **BPF's** can **be** used to achieve the narrow 1 **kHz** bandwidths needed. At this point the signal splits three ways into the blocks Tau-Dither code tracker, Doppler Scan/Track and Data demodulator. The Phase Modulation select switch is used for providing different signals to the phase modulator for the 2nd IF LO. All except the Code w/Dither position are used for testing only.

You might be wondering where the AGC is in this design. There isn't any. The receiver runs wide open. AGC is problem due to the C/A code spreading. To have **AGC** it would have to become active AFTER the **L1** signal is correlated which means that a switching scheme would be needed. This is not that difficult but its probably better left to a computer to decide on AGC levels. The receiver works without it so why not?

A **Word on IF Selection**

The **IF's** as implemented in this design are less than optimum. They came about in sort of a evolutionary way. I had some oscillators that were close, the simulator I built made some choices for me etc. The choice of the 28 MHz 1st IF was based primarily on existing designs for the ham band at 1.3 **GHz** which used a **28MHz** 1st IF. Also just the abundance of circuits in the Ham literature **at 28MHz** influenced me. The choice of the other **IF's was** based wrongly on my early attempts to make things multiples of the code clock. Not only is this not necessary you probably are asking for trouble doing this. Needless to say the design still worked and that is what counts!

Detailed Description of Receiver

The rest of this paper will be devoted to the details of the **L1** receiver. I will start at the antenna and work through to the data demodulator.

The Antenna

The antenna is a quadrafilar type taken straight from the ARRL Antenna Book, 15th edition, pages 20-1 to **20-7.** The design has good half hemisphere coverage which is exactly what is needed for a GPS receiver. The dimensions and other details of the antenna as built are given in figure 9. If you build this antenna make sure it is twisted the right way! This antenna has a gain of about 3 **dB.** It also is a fairly good match to **50** ohms.

The **Preamp**

Figure 6 shows a block diagram of the preamp. The first gain stage is a NEC Gasfet 32083. This FET has a gain of about 19 **dB** and a noise figure of 0.35 **dB** at 1575 MHz. The bias design of this fet was taken from The 1987 ARRL Handbook, pages 32-7. The input matching network is my own design. A lower cost FET such **as** the NEC NE720 or **NE710** could be used here and not compromise performance. The element that must be tuned is the inductor in the input matching network.

Tuning consists of deforming the turns while observing gain and noise figure. Tuning for maximum gain will also work at the expense of a slightly higher noise figure, but still acceptable performance.

Following the GasFet gain stage is a double tuned BPF. The bandwidth of this filter is approximately 40 MHz. The two air variable capacitors are tuned for max gain at 1575 MHz. The small wires serve as a capacitor coupler between resonators. The insertion loss of this filter is about 2.5 dB.

After the BPF are two gain stages using the MCL MAR-8's. These RF gain blocks are easy to use and relatively cheap. There is no tuning associated with the these two stages. These two amps combine for about 30 dB of gain.

Figures 7 and 8 give the construction detail of the preamp. It is constructed on double sided G-10 board. It is one of the few places where I used printed circuit techniques. The entire circuit is mounted in a custom made aluminum box. A SMA connector is used for the antenna input and a N type for the output to the RG-214.

The overall performance of this preamp is +46 dB gain with a noise figure of 1.0 dB (1.6 dB if tuned by gain alone). This is acceptable but it could be better. The input match to the FET needs improvement as does the BPF.

Crystal Down Converter

The signal from the preamp is fed via RG-214 to the down converter. The cable has 6 dB of loss. In reference to figure 2 the RF input from the preamp first passes through a interdigital BPF to aid in image rejection. The detail of this filter is shown in figure 10. This design is a modification of the design in the 1987 ARRL Handbook, page 32-23. The filtered RF and LO signals are applied to a MCL DBM TFM-11 to convert to the first IF of 28.644 MHz. The IF is then passed to a tuned amplifier that has a gain of 55 dB and bandwidth of 3 MHz. The details of this amplifier are shown in figure 11.

LO generation consists of a 28.644 MHz xtal oscillator followed by a X54 multiplier chain to achieve the LO frequency of 1546.776 MHz. The LO has a power level of about 7 dBm. Figure 12 shows the two spectrums of the 1540 LO. One shows the harmonic content and the other close in purity. The doubler and the two triplers to 515 MHz were built dead bug style on a 4 by 8 inch piece of two sided G10 board. Each stage was enclosed in small shield box soldered to the board with individual +15 feed throughs to minimize coupling. The filters were also enclosed in small shield boxes.

Figure 13 shows the circuits of the doubler and the two triplers with detail on filter construction. Layout follows the schematic using dead bug construction techniques. The doubler design is taken from Solid State Design For The Radio amateur P. 44. The last tripler to 1540 MHz is done on a separate 2 by 6 piece of G10. The input is fed from the 515 tripler via RG-74. This allows the circuit path to be broken for separate tuning/testing. The 515 to 1540 tripler uses a MAR-8 for the X3, an interdigital BPF to select the third harmonic and a MAR-4 to bring the output to power up to approximately. 7 dBm. The printed circuit pattern in negative is shown in figure 15. Circuit layout and detail of the interdigital filter is shown in figure 16. The interdigital filter is a modification of the design used in the

1296 **MHz** transverter in the 1987 ARRL Handbook P. 32-17. The tips on construction and tuning apply but the dimensions given in figure **16** must be used. I used end covers on the filter box which are not used in the Handbook design. Figure **17B** shows the xtal downconverter system.

A buffered 57.288 MHz output is picked off the 28.644 MHz doubler. This is used for testing but could also drive the dividers to generate the 2nd and 3rd **LO's.** This method would still need some sort of VCO for the 4th IF to allow for Doppler tracking.

If a 28.64 MHz VCXO is substituted for the fixed xtal oscillator the 4th LO could **also be** generated from this oscillator. This approach would eliminate the need for the additional oscillator and allow the 28.64 VCXO to handle Doppler tracking. The design used for the 10.23 code clock VCXO could be modified for this purpose.

28.644 **MHz XTAL** Oscillator

The circuit for the oscillator is shown in figure 17A along with layout. The crystal was obtained through ICM, Oklahoma City, OK. The oscillator could benefit from **a** temperature controlled oven as it can drift ± 20 HZ. This shows up as undesirable Doppler which eats away at the Doppler margin. Another undesirable is that this frequency is the same **as** the first IF. If any of the 28.644 makes it through the multiplier chain (and some does) it will appear in the 28.644 **MHz** IF. This is not as bad as it would first appear. The high gain of the preamp helps here as does the C/A code which **as** mentioned earlier will reduce any CW by 35 **dB.** A 57.288 MHz oven controlled overtone oscillator would solve both problems.

2nd **IF/Correlator**

The 28.644 MHz IF is fed to a DBM (MCL SBL-1) that does the correlation and down conversion to the second IF. The correlation is performed by phase modulating the LO drive. Phase modulation is done using a DBM (MCL SBL-1) driven at the I port by the C/A code. After the phase modulation the LO is BPF to limit the spectrum. As mentioned above when the receiver generated code is lined up within two chips the code on the **L1** signal the second IF will be present, otherwise noise.

The 22.9 MHz LO is derived by dividing the **114.613** VCXO output by 10 and then filtering to get the second harmonic. This is done using the ECL counter **MC10136.** The details of the circuits for the **2nd, 3rd,** 4th **IF's** and associated **LO's** is shown in figure 18.

The VCXO and the ECL dividers are mounted in a shield box. The ECL parts are super glued with legs flattened to **G10** board. Connections should be short. The Pulse stretcher is used to lengthen the pulses from the MC10136. The rest of the 2nd IF generation circuitry is mounted in a small shield box. To drive the DBM phase modulator **7414** and **74128 are** biased negative with respect to ground. This provides the bipolar drive signal necessary for BI-PHASE or BPSK modulation. The rest of the circuit is fairly straight forward and layout follows schematic with **"dead bug"** methods of construction on **G10** board.

The **MRF 901's** used in both the 2nd and 3rd **IF's** are overkill and

2N2222A's or equivalent will work fine although the bias resistors may have to be changed.

3rd and 4th IF Generation

Nothing remarkable here just standard down conversion. The details are shown in figure 18. Construction is "dead **bug**" on **G10** with the layout following the schematic. Each IF is mounted in its own shield box with SMA connectors for the inputs and outputs. The 4th IF box does not have the 20 **kHz** BPF inside. This is done at the C/A code Scan/Track and Doppler Scan/Track board.

114.6130 **MHz** VCXO

This is the only oscillator I did not build. I used a Vectron oscillator that had a 100 **kHz** FM range. The frequency stability requirements of this oscillator are mild due to the fact that it is controlled by the Doppler scan/track circuit. The frequency drift should be under 400 Hz. Its the **"pull"** range that is hard to come by. The oscillator used should be able to be pulled at least 40 **kHz** at **114** MHz. This oscillator can be replaced by making the 28.644 xtal oscillator a VCXO. See above under crystal downconverter.

Operation of the Tau-Dither C/A Code Scan/Track System

Figure 19 shows the block diagram of this system. The purpose of this system is to search for C/A code alignment and once found keep it there. Both functions are implemented by controlling the code clock frequency via the VCXO. The code clock VCXO is driven either by a constant voltage for Scan or a varying voltage for Track. An analog switch chooses between the two. When the switch is in Track position the system is said to be **"closed loop".** When in the Scan position the system is **"open** loop? Various waveforms and spectrums are shown accompanying the block diagram of figure 19. Some waveforms are open loop others are close loop. The open loop waveforms are marked with an asterisk.

Open **Loop Operation**:

In order to understand closed loop operation it is first necessary to understand open loop operation. In the open loop mode the code clock VCXO is held at a constant frequency offset from 1.023 MHz, the zero Doppler code rate. This frequency difference, about 10 Hz, causes the receiver generated code to **"slip"** by the code on the **L1** signal. The time it takes for the two 1023 bit codes to make **a** complete pass is **N/DF** seconds; where **N=1023** and **DF=10Hz** the frequency difference between the two code clocks.

Ignoring the effect of the Dither for now lets look at what occurs as the two codes slide by each other. As the two codes slip they will come to point where they **"correlate".** Correlation is when the two codes are within two chips of alignment. As correlation occurs the 20 **kHz** IF will start to appear at the output of the BPF. Before correlation the output of the BPF is just noise. The 20 **kHz** IF doesn't appear all at once, rather it builds in amplitude reaching a peak when

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the two codes are in perfect alignment. As the two codes continue to slip the **20 kHz** IF amplitude decreases until we are back to our noise output from the BPF. This process gives rise to the characteristic triangular shaped correlation pulse at the output of the **Full** Wave Detector. The width of this pulse is given by **2/DF,** where DF is defined as above.

Now lets look at the effect of the Tau-Dither. Tau dither is used to generate a voltage that can be applied to the code clock **VCXO** as to keep the codes in **"lock".** It does this by determining which side of the correlation pulse the receiver generated code is on and how far it is from the peak point. If we know which side of the correlation pulse we are on we can determine if the receiver generated code should be advanced or retarded with respect to the received code. Knowing how far off we are tells us how far we need to move the code.

This information is generated by "dithering," or switching, between two versions of the receiver generated code. One version is delayed the other is not. The delay used here is about **1/2** microsecond or **1/2** chip. As the two codes slip through correlation the dither switching induces AM on the 26 **kHz** IF. The frequency of the AM is the same **as** dither clock frequency. The amplitude of this AM increases to a maximum **and** then decreases to zero when the codes are in alignment. As the two codes continue to slip it again grows and diminishes to zero as we pass the correlation point. This **"double hump"** waveform can be generated by detecting the output of the dither BPF. This is shown in the block diagram but it is not used or needed in the actual circuit. At the midpoint of the double hump, at code alignment, the induced AM goes through a 180 degree phase shift. The phase shift contains the advance/retard information while the amplitude of the AM contains the "how **far"** information. The AM and its 180 degree phase shift at code alignment is caused by the triangular shape of the correlation pulse.

The dither induced AM is **picked off"** the full wave detected **20 kHz** IF with a BPF tuned to the dithering frequency. The dither AM is now multiplied by the dither clock reference. This recovers both the phase and amplitude information simultaneously. The output of the multiplier is **lowpass** filtered to give the **"discriminator"** error output. The 180 degree phase change causes a polarity reversal which produces the **"S"** shape discriminator output. We now have voltage whose polarity tells us whether to advance or retard our code and whose amplitude tells how much.

The low pass filter after the multiplier serves the same purpose as the loop filter in the more familiar phase locked loop. Much of the analysis of the code loop can be done using the tools from phase locked loops with slight modifications.

Closed **Loop** Operation:

When correlation occurs the carrier detector senses the presence of **the** 20 **kHz** IF and flips the switch from **Scan to Track.** The code clock VCXO is now being controlled by the error voltage from the discriminator. The discriminator voltage constantly **"pushes"** the receiver code in the proper direction so **as** to keep the two codes in lock. When the discriminator output is positive the code should be advanced, or lower the VCXO frequency. Just the opposite for negative

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voltages. In this manner the code clock VCXO is frequency modulated to keep the codes in alignment.

Getting a feel for the code scan/track process is best done with the aid of **L1** simulator. With the simulator the Ll code and the receiver code can be displayed on a two channel scope. By triggering on either the **L1** or receivers code epoch that code can be made to **"stand still"** on the scope. The other code will move across the screen in the direction determined by the sign of the frequency difference and at the rate determined by the magnitude of the frequency difference. If the loop is held open all the open loop waveforms can be observed as the two codes slide through correlation.

If we allow the scan/track switch to operate we can observe the transient and steady state behavior of the code track process. In steady state the tracking jitter can be measured.

Seeing the movement and dynamic properties of the **scan/track** system on a scope is hard to beat for getting a handle on this **tricky** problem.

C/A Code Scan/Track Circuit

Figure 20 shows the schematic diagram of the code scan/track circuit. This is a direct implementation of the block diagram of figure 19 with the exception of the dither detection which is omitted as stated above.

20 kHz IF Detector:

This is a full wave detector. LF 356 op amps are used for there high slew rate. This circuit was taken from P. 241 of the OP **Amp** Cookbook by Walter Jung, 3rd ed.

Carrier Detector:

The Carrier Detector consists of a **LPF/Threshold** detector, 10 turn pot, retriggerable one-shot, an OR gate and a LED. The one shot/OR gate are used to **debounce** the threshold detector output by extending the time that the analog switch is set to **"track".** The LED is lit for a carrier level above threshold. Threshold is set by the 10 turn pot.

Dither **Bandpass** Filter:

A single op amp active filter taken from P. 154 of the Active Filter Cookbook by Don Lancaster. This circuit has a Q of about 5. Because of the low frequency of the dither signal 741 type op amps work fine here. The filter is tuned to about 200 Hz. See below.

Four Quadrant **Multiplier/LPF**:

I used the Exar 2208 multiplier though any four quadrant multiplier would work due to the low frequencies involved. The details of operation and proper connections can be found in the 1988 Exar data book. A simple RC network at the output of the multiplier serves **as** the loop filter. The values of R and **c** will greatly effect code

tracking performance.

<u>Analog Switch/Amplifier</u>:

I used a MC14051 CMOS analog switch for the scan/track selection operation. Other switches could be used, even relays, with proper circuit modifications. This is a one-of-eight mix that is used as a SPDT switch. The other inputs are grounded. This switch can only handle plus or minus 5 volt signals. Because of this a 741 gain stage is added after the switch. The switch may be damaged if inputs exceed plus or minus 5 volts.

C/A Code Tau-Dither Loop Trade-Offs

The C/A code loop is a feedback loop and like all such loops there are trade offs in the design. The selection of the dither clock frequency is bounded by the IF bandwidth and by the need to "measure" the code error as frequently as possible. The maximum scan rate is limited primarily by CNR which in turn is related to IF bandwidth. The remaining "jitter" on the code lock is affected by the CNR, the loop filter, IF bandwidth, dither clock frequency and dither delay.

Using a Tau-Dither type of code tracking loop reduces the correlated IF amplitude by about 1.5 dB for this design. This loss gets larger for longer dither delays. Longer delays give better acquisition performance but result in more jitter.

Consequently the C/A code loop design is a trade off between the various requirements that are at odds with one another. The bibliography section lists a number of references on this topic.

Adjusting the C/A Code Scan/Track Circuit

There are a number of adjustments that must be done to the C/A Scan/Track loop for proper operation. The adjusting is done via ten turn pots. The schematic, figure 20, shows the location of each pot with the exception of the Dither frequency pot. With the exception of the Threshold pot all are of the miniature, screw type adjustment variety.

<u>Dither Frequency Adjustment</u>:

The dither BPF is not tuned but instead the dither frequency is changed to fall into the fixed pass band of the dither BPF. The dither clock is a 555 timer with a pot for frequency adjustment. The dither clock is part of the C/A code generating circuit and is shown in figure 25.

The tuning procedure is as follows: a simulated 20 kHz carrier is AM modulated with the dither clock. This could be done with a 555 timer and an AND gate. The output of the 200 Hz dither BPF and the 200 Hz dither clock are displayed on a two channel scope. Change the dither clock frequency until the two waveforms are either in phase, 0 degrees, or 180 degrees out of phase. This does two things; 1) It puts the dither clock frequency in the center of the Dither BPF 2) It aligns the PHASE of the detected dither AM with that of the dither clock. This is important. It insures that the multiplication of the

dither AM and the dither clock is done properly. The 0 or **180** degree alignment depends on where the dither clock is picked off; either before or after a logic inversion. Figure 22 shows the dither clock tuning setup. This brings up another point. If you are having trouble **"locking"** try inverting the dither clock reference to the multiplier. This will invert the error voltage polarity so that advance is now a negative error voltage and retard is now a positive voltage. Or visa versa.

Code Clock Bias Adjustment:

The code clock VCXO only responds to positive voltages. Therefore a bias is needed to allow for bipolar drive. This is provided by summing a bias voltage with the error voltage from the multiplier. The bias voltage is set to approximately 6 V dc. This assumes the code clock VCXO is adjusted properly. To adjust the bias a good frequency counter is needed. It should be accurate to **± 5** Hz at **10.23** MHz. The MULTIPLIER OFFSET adjustment should be done before this adjustment. The adjustment is done as follows; disconnect the dither reference signal and ground pin 3 on the **XR2208** multiplier. This should force the output of the multiplier to zero volts. Ground the IF input also just to be on the safe side. Force the track mode by reducing the threshold adjust pot until the carrier detect LED lights. This connects the VCXO control point to the output of the bias summer. Now adjust the bias pot until the frequency of the code clock is **10.230000 MHz.**

Multiplier Offset Adjust:

This adjustment compensates for any **d.c.** offsets in the multiplier. Ground the multiplier inputs as detailed in the Code clock bias adjustment. Now adjust the multiplier offset pot until the voltage on pin **11** of the **XR2208** multiplier is zero volts.

Threshold Adjust:

Threshold adjustment is provided by a ten turn precision pot with a vernier scale. Adjustment consists of turning the pot until the carrier detect LED just starts to flicker and then backing off a little so that the LED goes out. This must be done with the entire system up and consequently is a measure of the noise floor. This sets the level at which the system will declare that a carrier is present and correlation is assumed. The vernier scale is important. It enables resetting the threshold to various levels and monitoring any increase/decrease in the noise of the system.

20 **kHz** BPF adjustment:

The 20 **kHz** IF filter is shown in figure 23. There are three identical active **BPF's;** Two are used for the Doppler tracker and one is for the **20 kHz** IF. The center frequency of these filters is adjusted by a 10 turn pot. The adjustment of the IF filter is done at the same time as the Doppler filters. The details of the IF tuning are covered in the Doppler Scan/Track section.

C/A Code Generator

Figure 25 shows the schematic of the C/A code generator. This is a single code version of the generator shown in figure 2. Six **7495** four bit shift registers are used to implement the two 10 bit shift registers shown in figure 2. It is hardwired for satellite vehicle 9, tap points 3 and **10.** With the addition of some exclusive or gates and switching logic other codes could be generated.

Two versions of the code are generated. One delayed, one not delayed. The delayed code is the result of feeding the on time code through eight **74L04** inverter gates. This is about a **1/2** microsecond delay or 1/2 of a chip. These two versions are switched back and forth to produce the dither code. The dither clock is a 555 timer followed by a divide by 2 for square wave output. The dither frequency adjust pot is set as described above.

In addition to the dither code three other waveforms can be used for phase modulation of the 2nd LO. The three are code clock, on time code and CW (no phase mod.). These are use for testing purposes only. The 74153 is used to select one of these modulations by the setting of **S1** and S2, the phase modulation select switches.

Some method must be used to reset the generator to the all ones state. This is done by the code reset button. After **being debouced by** the two AND gates it is synchronized to the code clock by the D **flip-**flop 7474. The input to the shift register is held high by this **synced** pulse. This loads the register with all ones.

The C/A all ones state or epoch is generated by **AND'ing** all ten output bits of the 10 bit shift register. Two 4 wide **7421 AND** gates and two 2 wide 7408 AND gates are used for this function. The output is a 1 **kHz** pulse train.

C/A Code Clock VCXO

The C/A code clock is a 10.23 **MHz** VCXO followed by a divide by ten to produce the 1.023 MHz code clock. Figure 26 shows the schematic of the code clock generator. The VCXO is ovenized to reduce frequency drift. This oscillator will drift less than 2 Hz **at 10.23 MHz.** VCXO pull is about 250 Hz. This range can be increased by increasing the cap in series with the MV 209 diode.

Following the oscillator is a low pass filter used to reduce the upper harmonics. A MAR 3 is used as a buffer amp and a pick off point is provided for frequency monitoring. A 74160 is used to do the divide by ten operation and the 1.023 MHz is sent out via the 7404 inverter.

The oscillator/filter/buffer were built dead bug style on a 1 **1/2** X 3 inch **piece** of **G10.** This was fitted with **a** tin cover. The heating resistors were **epoxyed** to the cover. The completed oscillator **was** then put in **a** tight fitting Styrofoam box. The power, heater and 10.23 MHz outputs were brought out of the box. RG-74 was used for the 10.23 MHz outputs.

Heater control is provided by comparing the **voltage** from the LM336, a precision 2.5 volt reference, and a LM335 temperature sensor. When the divided voltage from the LM335 is below 2.5 volts the heater is **turned** on. When above its off. The heater is made of four 220 **ohm,** 1/2 watt resistors in parallel. The set **temperature is** controlled by the **10k** ten turn pot.

Code Clock VCXO Frequency Adjustment:

Frequency can be adjusted by the control point to the tuning diode, the piston trimmer on the oscillator board and to a lesser extent the oven temperature via the ten turn pot. A good frequency counter is needed to adjust this oscillator, accurate to within a few Hz at 10.23 MHz.

The heater must be adjusted first. Prior to applying power to the heater control adjust the Temp. Set Pot for lowest temperature, i.e., wiper at the top. Now apply power and slowly bring up temperature to about 125 **F** or about 3.2 V dc at the temp sensor. Once the temperature has stabilized adjust the frequency of the oscillator about 100 Hz BELOW 10.23 MHz using the piston trimmer. It is set low to allow for the **d.c.** bias added to the code error signal. If the trimmer cannot bring it into tune try changing the oven temp a little and readjust piston trimmer .

If a higher code scan rate is desired set the oscillator even lower. The limit here is the **total** pull at the control point which as mentioned above is about 250 Hz. With this range 180 Hz below should be feasible and would result in about the highest scan rate that could be used with this system.

The design for the oscillator was inspired by designs found in the 1988 **ARRL** Handbook. The heater control circuit came from the data sheet applications for the **LM** 335 sensor in the Linear Data Book from National Semiconductor.

Doppler **Scan/Track System**

As discussed above the narrow IF bandwidth of **1kHz** and the ± 7 **kHz** Doppler on the **L1** carrier make it necessary to do a Doppler scan and track operation. Figure 23 shows the Doppler scan/track sub-system.

Scan:

The scan function is implemented by letting the 8 bit UP/DOWN counter free run with the **UP/DN** input held low. The counter is driven by a **1.5 sec** period clock. The output of the counter is converted to analog by the DAC. This results in a sawtooth waveform with a 6 minute period coming out of the DAC. The output of the DAC is summed with a bias to account for zero Doppler. This is fed to the 114.613 **MHz** VCXO. In other words the **L1** signal is swept through all possible Doppler offsets by the VCXO until it **"falls"** into the Doppler filters. The range of the Doppler scan is determined by the voltage divider at the DAC output amp. The range as shown is about ± 5 **kHz.**

All three filters will have some of the signal in them since they are about **500** Hz apart and have approximately 1 **kHz** bandwidths. When this condition occurs in conjunction with correlation the carrier detect circuit is tripped. This activates both code and Doppler track circuits.

Track:

The output of the two Doppler filters is detected and low pass

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filtered. The comparator subtracts these two levels to determine which filter has more of the **L1** signal in it. In the track mode control of the Up/Down input of the 8 bit counter is switched to the output of the comparator. If the **L1** signal is more in the lower Doppler filter the comparator tells the counter to count up. If the **L1** signal is more in the upper Doppler filter the comparator tells the counter to count down. The output of the counter, when converted to analog by the DAC, keeps the **L1** signal centered in the 20 **kHz** IF filter.

The two D type flip-flops are used to sync the **UP/DN** and Carrier Detect signals to the 2 second clock pulses. The **UP/DN** LED gives a visual indication of which direction the counter is going. When tracking Doppler the **UP/DN** LED should toggle between high and low at about the 2 second clock rate. I used a Burr Brown 8 bit DAC but any 8 bit DAC should work.

Adjusting the Doppler Scan/Track Circuit

There are only two adjustments to the Doppler scan/track system. Doppler zero and the Doppler filters center frequency.

Doppler filter adjustment:

Figure 24 shows the schematic of the active filter used for the three Doppler filters. The filter is tuned via **R1** a ten turn miniature pot. A signal generator or 555 timer is needed as an input for tuning the filters. The lower Doppler filter is tuned to approximately **19.5 kHz.** The upper Doppler filter is tuned to approximately 20.5 **kHz.**

The middle Doppler filter, which is used for providing the 20 **kHz** IF to the code loop and data demodulator, is tuned by one of two methods. The first method uses a signal generator to find the frequency at which the comparator toggles. This is the frequency that the middle filter should be tuned to. This method will produce adequate results.

The second method uses a either a 1575.42 MHz RF or 28.644 MHz IF simulator. The middle filter should first be tuned by the first method so this really is the **"fine"** tuning part. Assuming a simulator is available connect a -40 **dBm** 28.644 **MHz** CW signal to the 1st IF input or a -120 **dBm** 1575 MHz **CW** signal to the preamp input. Set the phase modulation select switches to CW. This allows the CW to pass **"unspread"** through the system and no code lock is needed. Allow the system to track the CW signal. Using **a** voltmeter or scope tune the middle filter for maximum voltage or amplitude. This method closes the loop and should produce a more accurate result.

Doppler Zero:

The VCXO may not be set exactly to the frequency that would put the **L1** signal in the center of the 20 **kHz** IF filter when **L1 has** zero Doppler on it. A bias voltage is summed with the DAC output to compensate for this error. The VCXO does not have to be set closer than ± 200 Hz.

There are many ways to adjust the VCXO for zero Doppler. The most straight forward is to use a frequency counter to measure the VCXO frequency and to adjust the bias pot accordingly. If there is no

offset in the oscillator used in the downconverter then the VCXO
frequency for zero Doppler is **114.6130 MHz.** The voltage from the DAC
must set to zero to do this adjustment. The switch on the plus input
of the bias amp is used for this purpose.

Acquisition Times

    The combined requirements of scanning the C/A code and Doppler
lead to some questions about how long it takes acquire the **L1** signal.
Assuming that the scan rates and bandwidths remain constant CNR is the
determining factor. Larger **CNR's** result in shorter acquisition times
while smaller **CNR's** lead to longer ones. For a CNR of about 20 **dB** this
system will have a average acquisition time of 5 minutes. This time
could be decreased by increasing the scan rates. The code scan rate
would have to be increased before the Doppler scan rate can be
increased. The scan rates used here are slow compared to what could be
used.

Data Demodulator

    A block diagram for the data demodulator is shown in figure 27.
The Schematic is shown in figure 28. This design is based on **a** block
diagram found on **P.** 211 of Phase Locked Loops by Roland Best.
    After the C/A code is removed a 50 BPS data stream remains. This
is present on the 20 **kHz** IF as **BPSK** modulation. The first step in the
demodulation of this data is to hard limit the 20 **kHz** carrier. This
removes any amplitude variation. The limited IF is now fed to a CD4046
PLL chip. The PLL responds to PHASE changes on the data with an
impulse, not a pulse. The impulses occur at every phase transition.
Since there are two phase transitions per data bit, one for the rising
edge and one for the falling edge, there are two impulses per data
bit.
    The impulses can have either positive or negative polarity and
can flip arbitrarily. To make all impulses have a positive polarity a
full-wave rectifier is used. This is done with a couple of LF356
opamps and four diodes. This design is lifted from P. 241 of the OP
Amp Cookbook by Walter Jung, 3rd edition. After rectification a **non-**
inverting gain of 3 is used to increase the impulse amplitude.
    Now a 7414 is used to clean up the impulses and bring them to TTL
levels. A **oneshot** with a output pulse width of 8 milliseconds is used
to stretch the impulse into a pulse and add some noise immunity.
    The data pulse train is now divided **by** two in order to eliminate
the two pulses per bit and to **"square it up".** This is done with a 7474
D-type flip-flop. The Q output is taken as the demodulated data
stream. Now that we have the data signal we still need to know when to
sample the data waveform. The data clock is needed.
    The data clock can be reconstituted by dividing the 1 **kHz** C/A
code epochs **by 20.** This gives the needed 50 **Hz** data clock. This is
done using a 74160 decade counter for the divide by ten and a 7474 for
the divide by 2 to get the divide by twenty. This circuit is shown in
figure 28.
    The only adjustment in the data demodulator is the PLL **VCO**
frequency. The free running frequency of the VCO should be 20 **kHz, the**
IF frequency. Adjustment can be done when tracking a satellite. When

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the Doppler tracker settles down and is tracking the satellite monitor
pin 9 of the PLL on a scope. Now adjust the VCO frequency via the 5
kohm pot until the D.C. level on pin 9 of the PLL is about zero volts.
This should insure that the free running frequency of the VCO is close
to 20 kHz.

Another method is to use a signal generator to generate the 20
kHz IF. This is fed to the Doppler filters and the frequency varied to
find the point at which the Doppler comparator toggles. Now adjust the
PLL VCO as above.

The performance of the data demodulator could be better. Signals
with CNRs below about 15 dB will produce bit errors on the order of 1
in 600 or worse. Above this the performance is quite acceptable and
good results were obtained. The detected IF level that I used as a
threshold was about 2 volts.

Results

The receiver was used to track and receive data from satellite
vehicle 9. The data was taken November 23, 1989 at approximately 3:30
AM PST. The satellite passed nearly overhead at this time. this
insured good signal strength. Figure 29 shows a elevation plot of
satellite vehicle 9 for Nov. 23 1989 at my latitude and longitude. The
afternoon occurrence was at a low elevation angle and did not provide
very good data but the receiver was still able to track it.

Figure 30 shows a recording of detected IF level and VCXO control
voltage from the Doppler tracker for the early morning occurrence.
Figure 31 shows the received data spectrum from the satellite on the
20 kHz IF taken at the afternoon occurrence. The Doppler plot shows
the sawtooth scan until the satellite is "locked on" by the receiver.
The detected IF slowly rises as the satellite comes up. Zero Doppler
is a little off due to some frequency drift in the downconverter. As
the satellite goes back down the Doppler increases to the point where
lock is broken. This is due to the drift and the fact that I was only
set up for about a ± 5 kHz range of Doppler. Given more Doppler range
the receiver should have tracked for about another hour. Once lock is
broke the Doppler goes back to the scan mode and the Det. IF shows
just the noise level. There is a brief "lock up" after the loss of
lock but it is short lived.

The Data

The data was read using a HP3270 computer that had an eight bit
input port. The clock was attached to bit zero and the data to bit 1.
The data line was read on either the rising or trailing edge since it
was not certain at the time which would give the best results. It
turned out that the trailing edge data was the good stuff.

Figure 32 is a sample of the data. The data is sent in 30 bit
words. Ten words make a subframe. There are five subframes for a full
frame of data. The first 8 bits of each subframe are the same. This is
the preamble. After the data was read into the computer a program was
used to "hunt" for the preamble pattern. When five preambles are found
that are 300 bits apart a "sync" is declared.

When the "sync" is found the program then sorts the data into 30
bit words and 10 word subframes. The subframe ID's are contained in

bits 20-22 of the second word in each subframe. The subframe ID's are printed in a column at the right margin. Both the inverted and non-inverted are printed as the program did not check for data polarity which can be arbitrary. The data polarity can be determined from the preamble. The polarity of the data shown is correct and the left hand column of subframe ID's is the correct one. Of course one could also tell by the sequence, i.e. 1, 2, 3, 4 and 5 etc, as they are sent in order. The right hand column of numbers is a count of the data bits as they where read into the computer.

The important item here is the preamble. When you see that pattern repeat every 300 bits you know you have the data! Figures 33 and 34A/B show some the internal detail of the data format. These figures were taken from the ICD-GPS-200 document.

This is as far as I have taken the data analysis. To go further requires a lot more programming and possibly computer control of the receiver.

Obtaining the ICD-GPS-200 Document

This key document is available from the GPS program office. A letter must be sent to the address given below stating name and purpose. Unfortunately they do not have to send you a copy! Although the document IS NOT classified the program office will decide on a case by case basis if the requesting party can be "trusted" with a copy. I could get no firm commitment on the qualifications needed to get the document, although I was told that if my address was in Moscow I would not receive a copy. Strangely, they did not object to the inclusion of the C/A Code Tap Point table and the Data Frame Format figures, the very information I found to be the most difficult to obtain!

The C/A code portion of the L1 signal is for public use. The GPS system was paid for and is owned by the people of the United States. Currently there are foreign and domestic manufacturers who are profiting from C/A code receivers. If the large corporations have access to system information shouldn't the experimenter and the entrepreneur?

GPS Program Office address and phone number:

Space Systems Division/MZEE
ATTN: Data Manager
Los Angeles Air Force Base
P.O. 92960, Los Angeles, CA
90009-2960 Tel 213-643-0880

Acknowledgements

I would not have been able to build this receiver without the many fine publications provided by the HAM radio people. In particular the ARRL publications. They had examples of real circuits that worked. I would also like to thank Todd Carstenson who wrote the data capture program and provided a source of encouragement. There are many people who added bits and pieces to this endeavor, librarians, co-workers, people in industry, etc, who I would also like to say thanks.

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LIST OF FIGURES MD **TABLES**

Figures:

Tables:

SIMPLIFIED MODEL OF GPS L1 GENERATION

FIGURE 1

C/A CODE GENERATOR

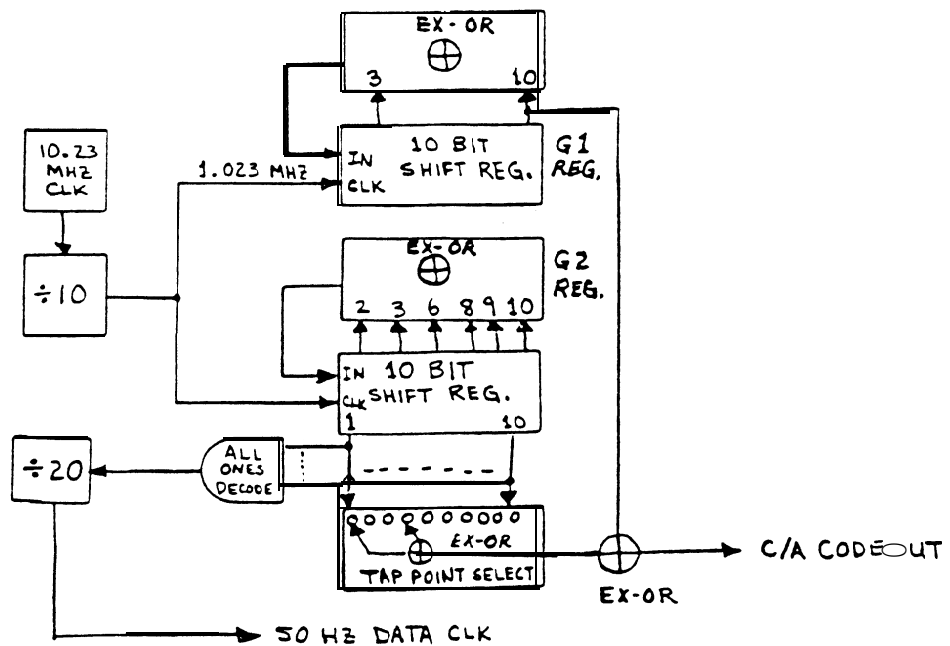**FIGURE 2**

FIGURE 3
L1 POWER SPECTRUM

TABLE 1
C/A CODE SHIFT REG. TAP POINTS

SV NO.	CPS PRN Signal NO.	Code Phase Selection		Code Delay Chips		first 10 Chips Octal	First 12-Chips Octal
		C/A (G2;)	(X2;)	C/A	P	C/A	P
1	1	2⊕6	1	5	1	1440	4444
*2	2	3⊕7	2	6	2	1620	4000
*3	3	4⊕8	3	7	3	1710	4222
4	4	5⊕9	4	8	4	1744	4333
5	5	1⊕9	5	17	5	1133	4377
*6	6	2⊕10	6	18	6	1455	4355
7	7	1⊕8	7	139	7	1131	4344
8	8	2⊕9	8	140	8	1454	4340
*9	9	3⊕10	9	141	9	1626	4343
10	10	2⊕3	10	251	10	1504	4343
*11	11	3⊕4	11	252	11	1642	
*12	12	5⊕6	12	254	12	1750	
*13	13	6⊕7	13	255	13	1764	
*14	14	7⊕8	14	256	14	1772	
15	15	8⊕9	15	257	15	1775	
*16	16	9⊕10	16	258	16	1776	
17	17	1⊕4	17	469	17	1156	
18	18	2⊕5	18	470	18	1467	
19	19	3⊕6	19	471	19	1633	
20	20	4⊕7	20	472	20	1715	
21	21	5⊕8	21	473	21	1746	
22	22	6⊕9	22	474	22	1763	
23	23	1⊕3	23	609	23	1063	
24	24	4⊕6	24	612	24	1706	
25	2s	5⊕7	2s	613	2s	1743	
26	26	6⊕8	26	614	26	1761	
37	27	7⊕9	27	515	27	1770	
28	26	8⊕10	28	516	26	1774	
29	29	1⊕6	29	859	29	1127	
30	30	2⊕7	30	860	30	1453	
31	31	3⊕8	31	861	31	1625	
32	32	4⊕9	32	862	32	1712	
**	33	6⊕10	33	863	33	1745	
..	34*	4⊕10	34	950	34	1713	
**	35	1⊕7	35	947	35	1134	
**	36	2⊕8	36	948	36	1456	
..	37'	4⊕10	37	950	37	1713	4343

'C/A codes 34 and 37 are common.
**PRN sequences 33 through 37 are reserved for other uses (e.g. ground transmitters).

FROM ICD-GPS-200
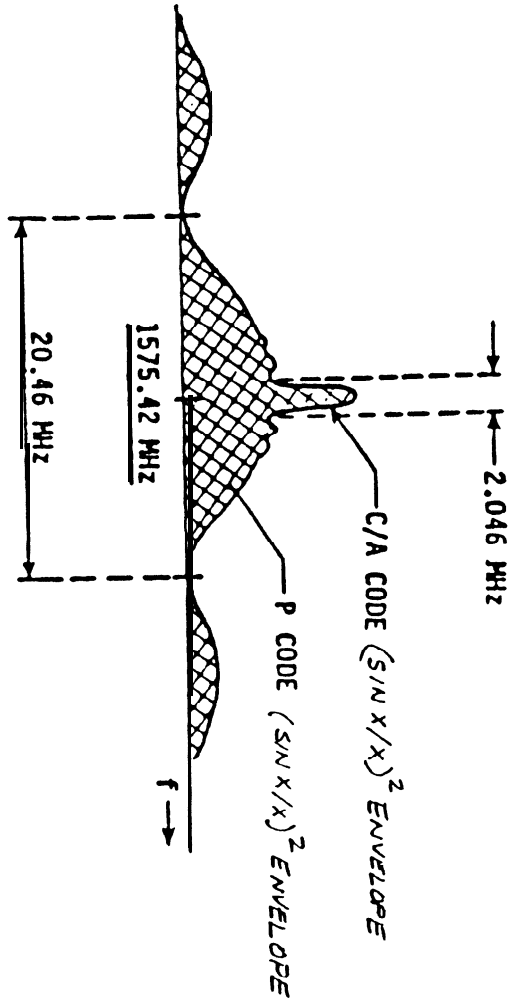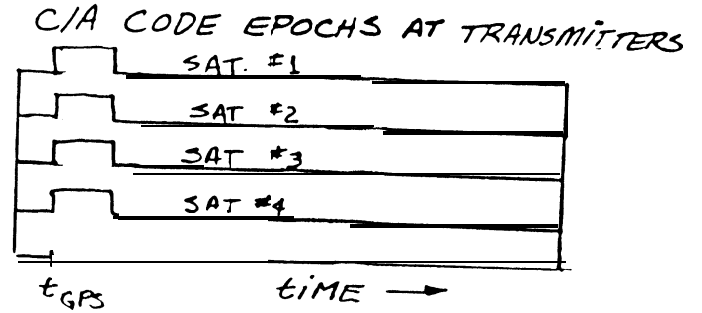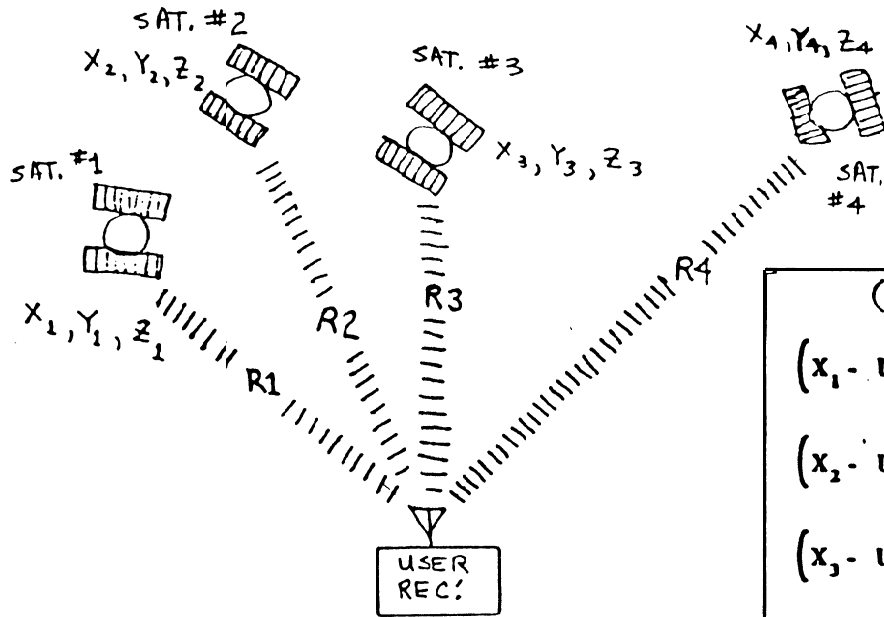* ACTIVE SATELLITES AT THE TIME OF THIS PAPER

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FIGURE 4.
POSITION MEASUREMENT

SAT. #2
X_2, Y_2, Z_2

SAT. #3

X_4, Y_4, Z_4

SAT. #1

X_3, Y_3, Z_3

SAT. #4

X_1, Y_1, Z_1

R2 R3 R4

R1

USER REC.

C/A CODE EPOCHS AT TRANSMITTERS

SAT. #1
SAT #2
SAT #3
SAT #4

t_{GPS} time →

MEASURE FOUR DELAYS & COMPUTE PSEUDO RANGES

ΔT1
ΔT2
ΔT3
ΔT4

t_0 time →
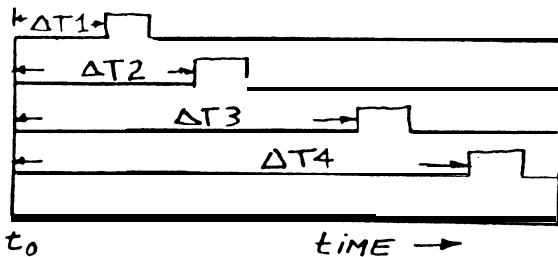
C/A EPOCHS RECEIVED BY USER ARE DELAYED BY PATH LENGTHS R1 - R4.

COMPUTE POSITION COORDINATES
(FOUR EQUATIONS WITH FOUR UNKNOWNS

$$\left(X_1 - U_x\right)^2 + \left(Y_1 - U_y\right)^2 + \left(Z_1 - U_z\right)^2 = \left(R_1 - C_B\right)^2$$

$$\left(X_2 - U_x\right)^2 + \left(Y_2 - U_y\right)^2 + \left(Z_2 - U_z\right)^2 = \left(R_2 - C_B\right)^2$$

$$\left(X_3 - U_x\right)^2 + \left(Y_3 - U_y\right)^2 + \left(Z_3 - U_z\right)^2 = \left(R_3 - C_B\right)^2$$

$$\left(X_4 - U_x\right)^2 + \left(Y_4 - U_y\right)^2 + \left(Z_4 - U_z\right)^2 = \left(R_4 - C_B\right)^2$$

SOLVE FOR USER'S POSITION COORDINATES $\left(U_x, U_y, U_z\right)$ AND CLOCK BIAS, C_B

C_B IS CLOCK BIAS RANGING ERROR
$$= C \Delta T_B$$

ΔT_B = USER CLOCK TIMING ERROR

PSEUDO RANGES
$$R1 = C \times \Delta T1$$
$$R2 = C \times \Delta T2$$
$$R3 = C \times \Delta T3$$
$$R4 = C \times \Delta T4$$

C IS SPEED OF LIGHT

FIGURE 5
GPS L1 DATA RECEIVER
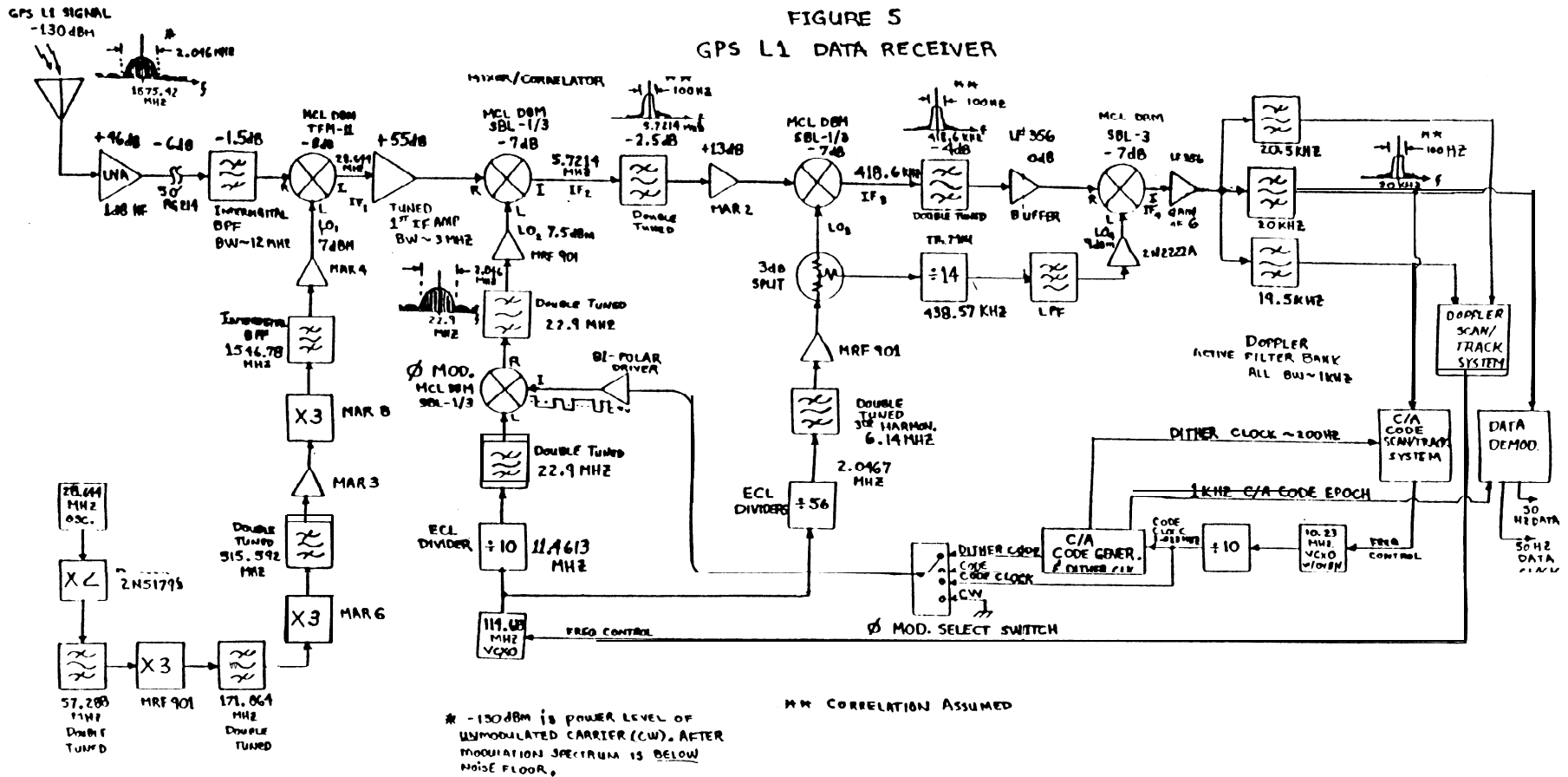
FIGURE 6
PREAMP BLOCK DIAGRAM &
SCHEMATIC

Block diagram:

L1 IN 1575.42 MHZ -130dBM → +19dB (NEC 32083) → -2.5dB (DOUBLE TUNED 1575.42 MHZ) → +15dB (MAR8) → +15dB (MAR8) → L1 OUT -83.5dBM

+46.5 dB GAIN
1 dB N.F.
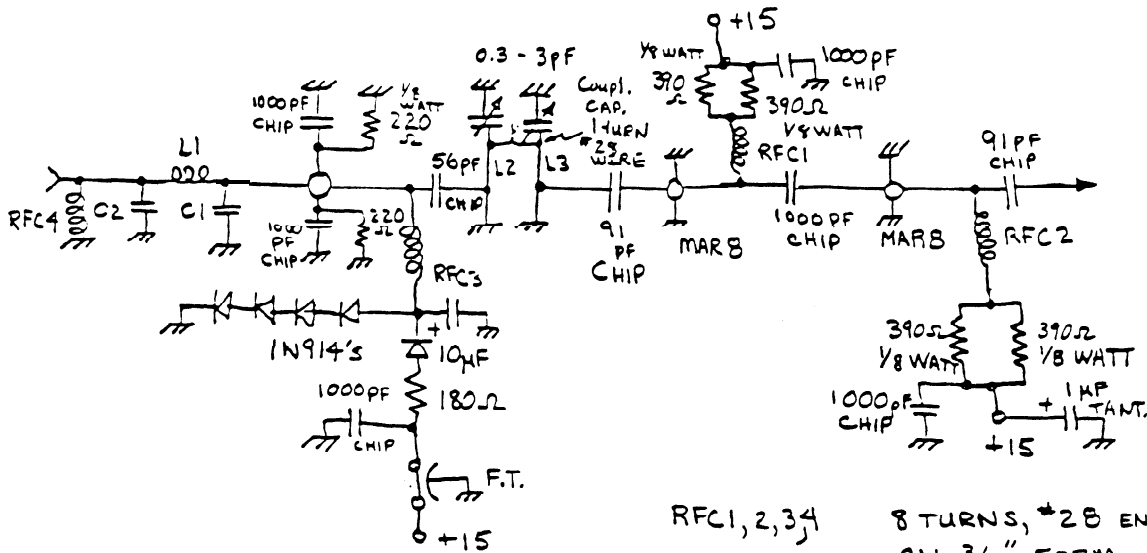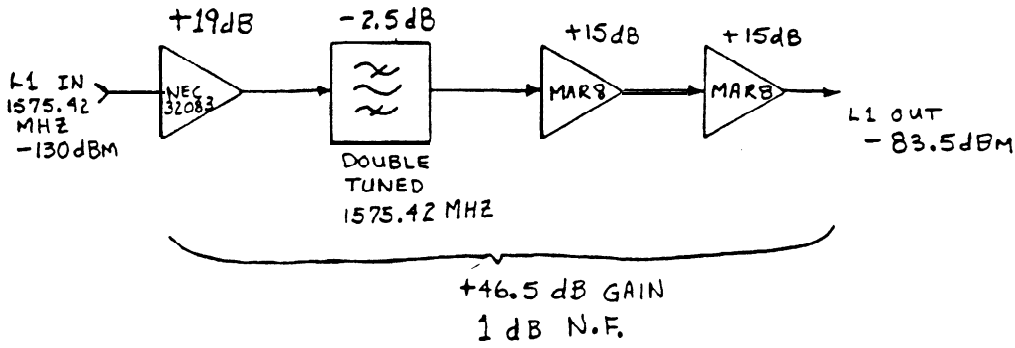
RFC1,2,3,4   8 TURNS, #28 ENAM. WIRE ON 3/16" FORM

C1   2.2 PF, CHIP

C2   0.3 PF, CHIP

L1   3 TURNS, #28 ENAM. WIRE ON #50 DRILL (0.07" DIA)

FIGURE 7
LAYOUT & ARTWORK FOR PREAMP

NEC 32083

IN

0

MAR8

0.3 - 3 PF PISTON TRIMMERS

NEC 32083

RFC4
220Ω ⅛ WATT

SMA

36 PF CHIP

C2 C1

220Ω ⅛ WATT

IN914

RFC3

10μF

IN

(4) IN914

180Ω 1 WATT

1000 pF CHIP

L2   L3

91pF

CHIP

MAR 8

+15 VDC F.T.

+15 UNDER to A

A

1000 CHIP

390//390Ω RFC1

OUT

1000 PF CHIP

91pF CHIP

TYPE N

MAR 8

RFC2

390//390Ω

1000 PF CHIP

1μF TANT.
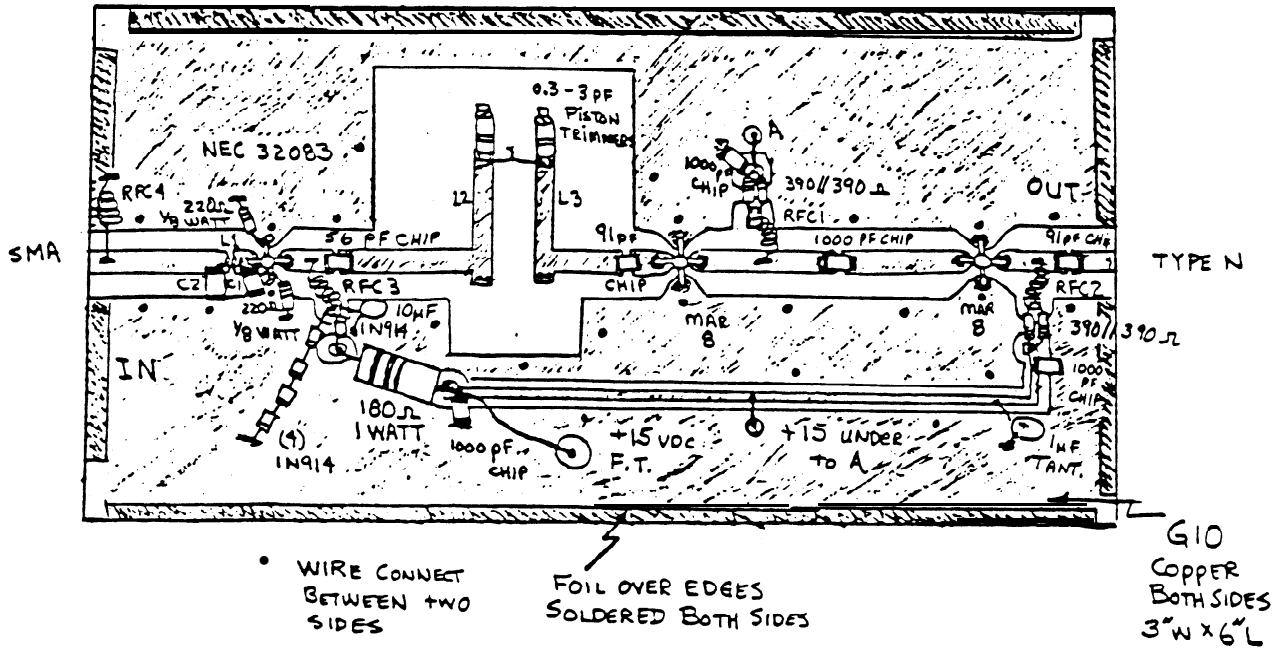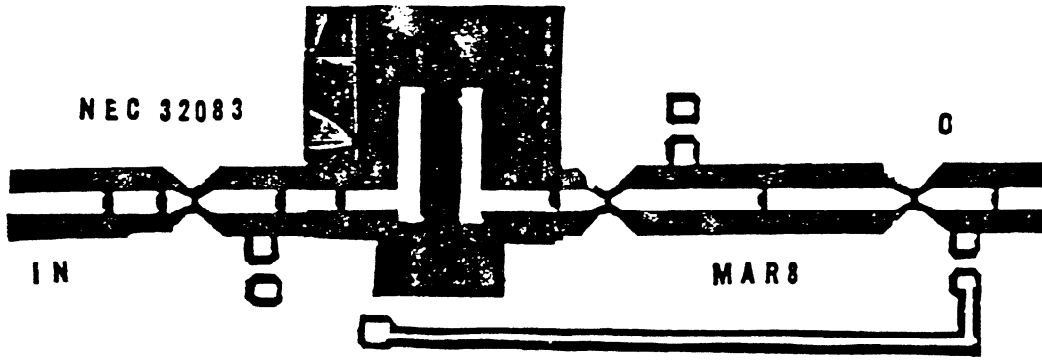
• WIRE CONNECT BETWEEN two SIDES

FOIL OVER EDGES SOLDERED BOTH SIDES

G10 COPPER BOTH SIDES 3"W x 6"L

BEND LEADS UP AND OVER

NEC 32083 GASFET

220Ω ⅛ WATT

L1

1000 PF CHIP

1000PF CHIP

220Ω ⅛ WATT
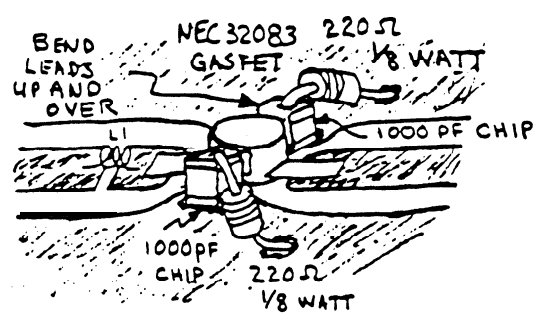
DETAIL OF NEC 32083
MOUNTING TO CHIP CAPS; C1&C2
ARE NOT SHOWN

5 15/16"

4-40

1/8" ALUM.

SIDE, 3/16" ALUM.

LID STOP

ANT
IN
SMA

LID
STOP

OUT
TYPE N (BULKHEAD)

4-40

CIRCUIT BOARD
TOP

TO
RG-214

2-56

4-40

+15 SMA

2 1/8"

6-32

6-32

13/16"

5/16" x 1/4" SHELF

1/16" ALUM.

4-40

SIDE VIEW

FIGURE 8

PREAMP BOX

3 9/16"

TUNING
ACCESS

SHELF
FOR BOARD

+15 SMA

CIRCUIT
BOARD
TOP

STOP
FOR
LID
5/16" x 1/4"

TOP VIEW.

END VIEW
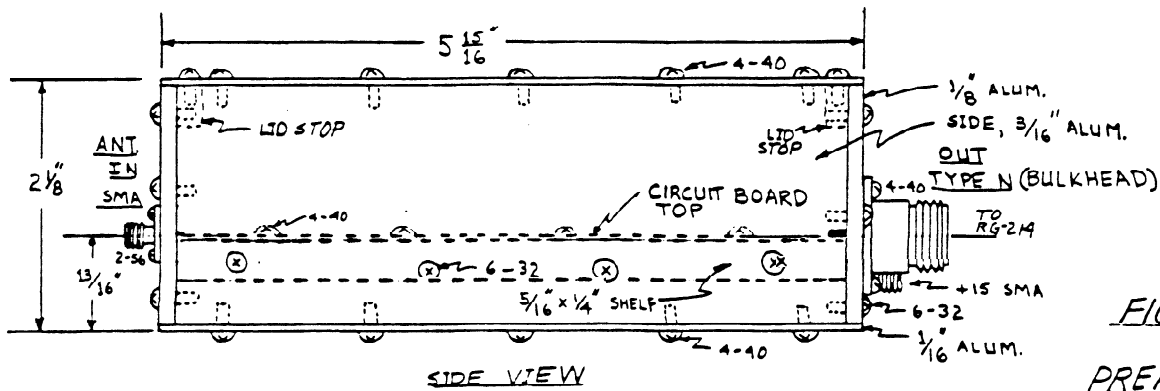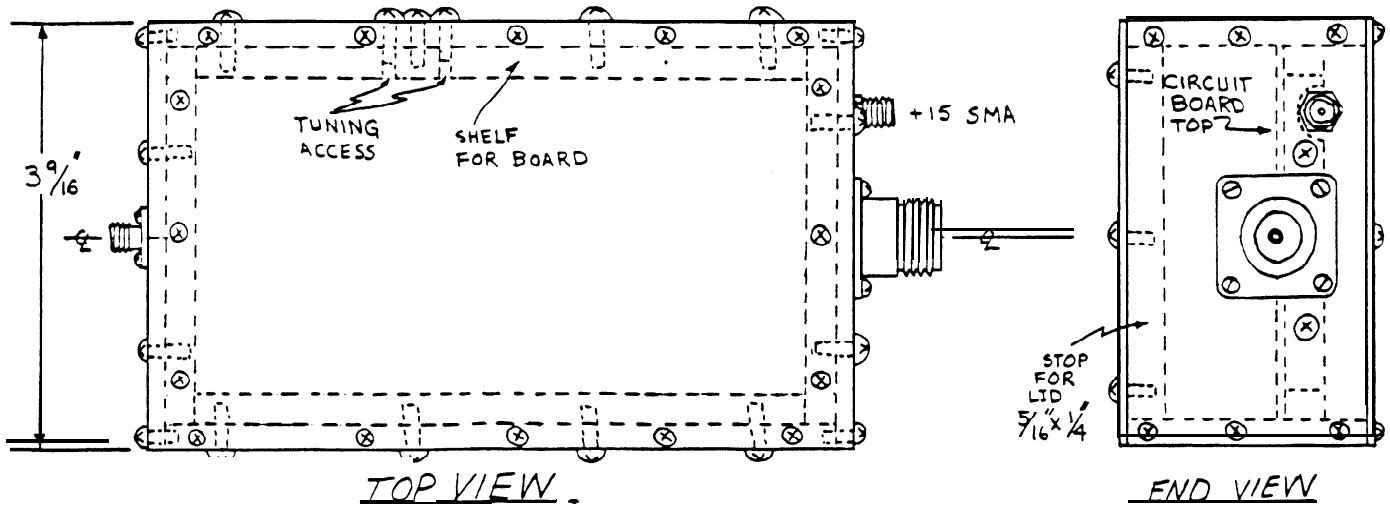
52

FIGURE 9

QUADRIFILAR ANTENNA - FROM ARRL ANTENNA BOOK, 15TH ED.

SIDE VIEW

DIRECTION OF TWIST

0.085 50Ω COAX

1.95"

1.78"

0.17"

#18 Solid Copper

1.16"

#18 Solid Copper

Cut Slot In Rod For 50Ω Coax - Fill With Solder

3/8" DIA. Copper ROD 7/10" LENGTH.

FEMALE SMA

1.3"

LENGTHS OF ELEMENTS

C1, L2	8.4"
L1, L3	7.6"

TOP CONNECTIONS
(VIEWED FROM TOP)

#18 SOLID COPPER

0.085 50Ω COAX

Solder Together

L1 & L2

L1

#18 Solid Copper

SOLDER CENTER COND. OF 50Ω COAX TO L1 & L2

SOLDER L3 TO OUTER CONDUCTOR OF 50Ω COAX

#18 SOLID COPPER

BOTTOM CONNECTIONS
(VIEWED FROM TOP)

#18 SOLID

SOLDER

L3

SOLDER

0.085 50Ω COAX

C1

L1 SOLID

L2

SOLDER

#18 SOLID

DRILL HOLES IN 3/8" ROUND FOR #18 SOLID WIRE, THEN SOLDER

FIGURE 10

.1575.42 BPF, INTERDIGITAL DETAIL*

10-32 SCREWS W/ LOCK NUTS

2 1/16"

1.7"

1.7"

1.7"

SMA

1/2"

1/4" x 1/32" Strip

1/8" DIA. HOLE

SMA

4-40 SCREWS

6-32 SCREWS

1 1/4"

12/16"

13/16"

1/4" DIA. COPPER RODS

BRASS OR COPPER PLATE

2 5/8"

6-32 SCREWS

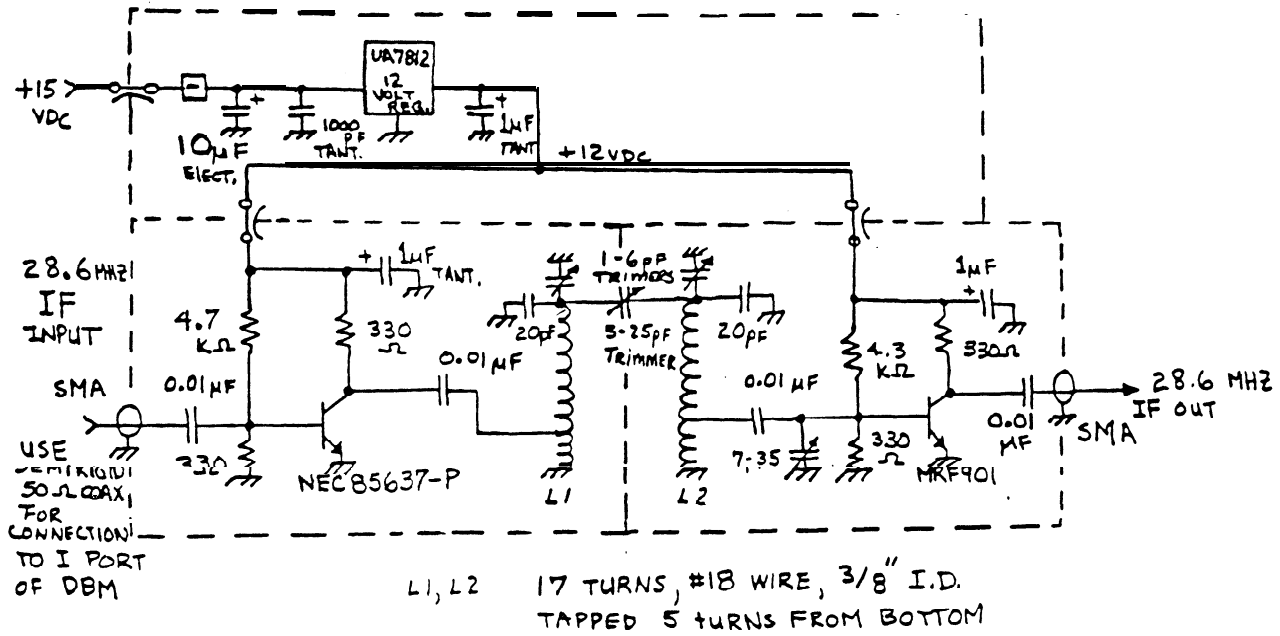6-32 SCREWS
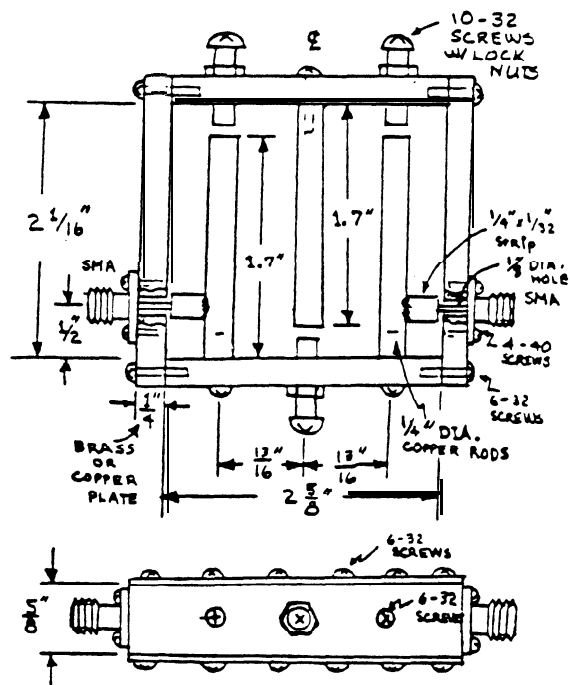
* SEE ARRL HANDBOOK 1988 OR VHF/UHF HANDBOOK, RSGB

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FIGURE 11
28.6 MHZ 1ST IF TUNED AMP. (55dB GAIN, 3MHZ 3dB B.W.)

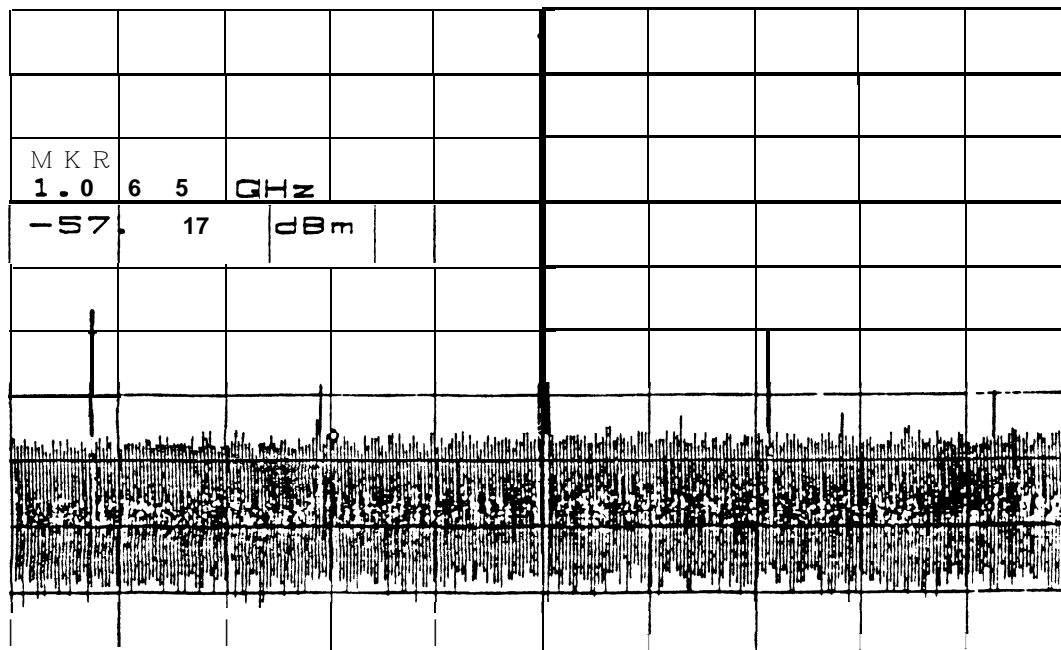L1, L2   17 TURNS, #18 WIRE, 3/8" I.D.
TAPPED 5 turns FROM BOTTOM

1ᵗ L.O.

ATTEN 20dB   MKR −57.17dBm
RL 10.0dBm   10dB/   1.065GHz

```
MKR
1.0 6 5  GHz
−57. 17  dBm
```

CENTER 1.547GHz   SPAN 2.450GHz
RBW 1.0MHz   VBW 1.0MHz   SWP 50ms

FIGURE 12
1ˢᵀ L.O. OUTPUT

1ᵗ L.O.

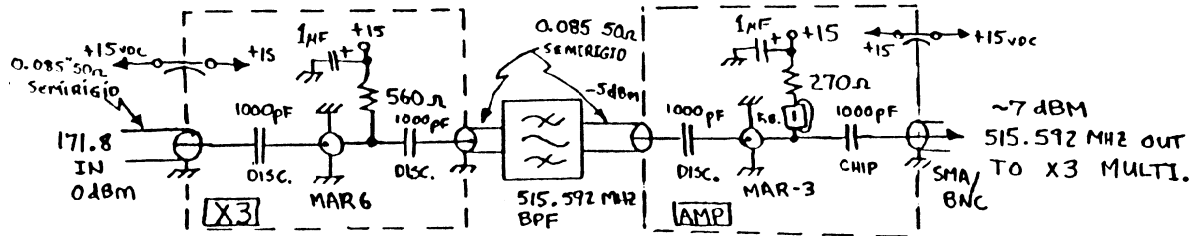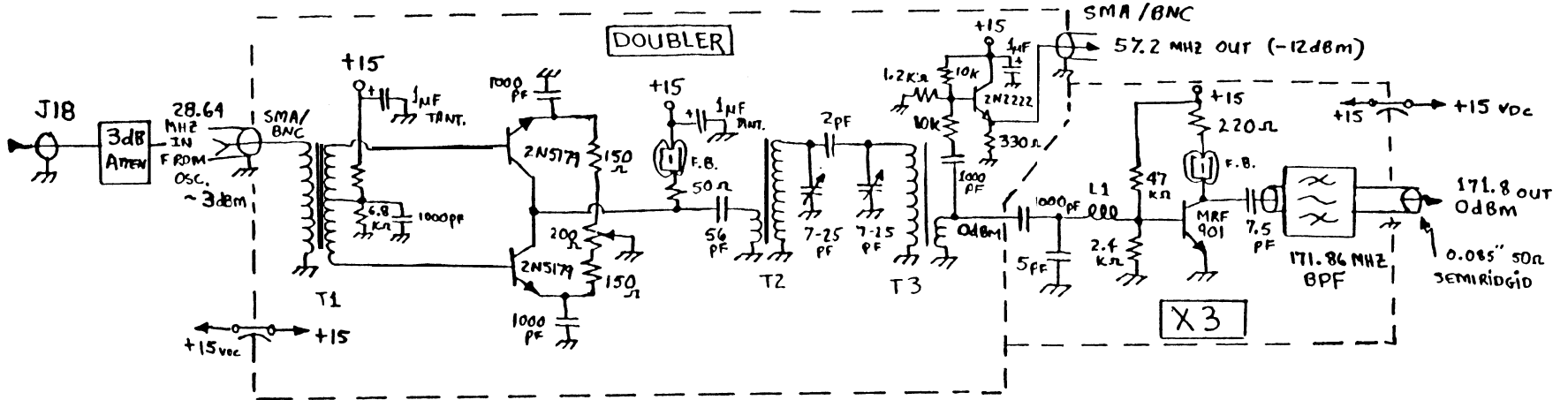ATTEN 20dB   MKR 6.67dBm
RL 10.0dBm   10dB/   1.546777369GHz

```
SPAN
5.000 kHz
```
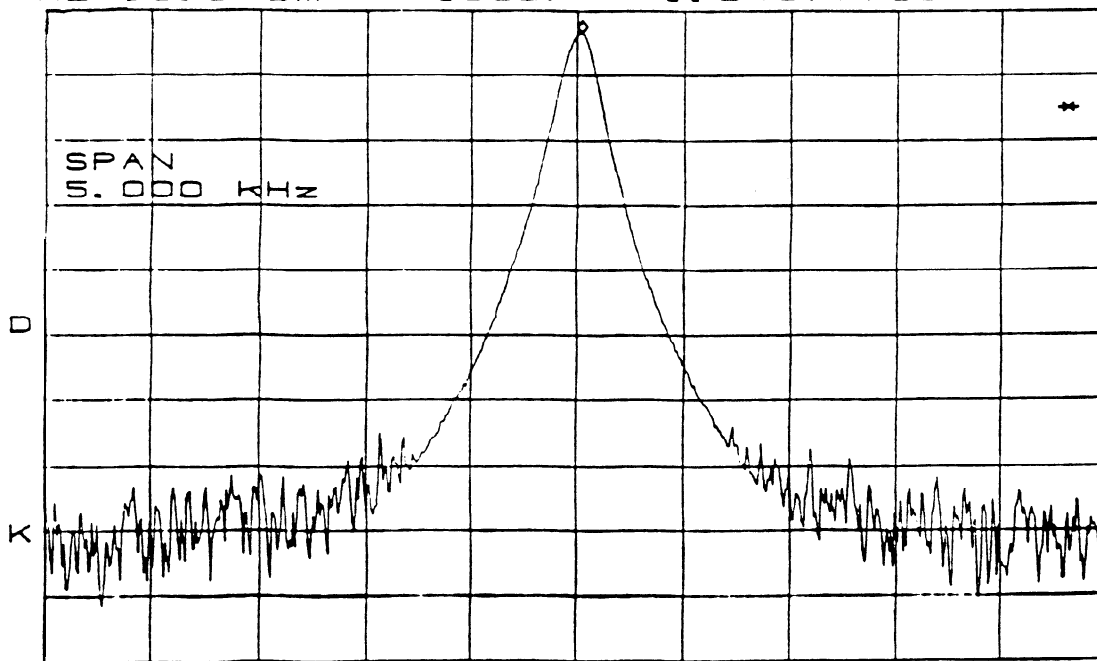
CENTER 1.546777369GHz   SPAN 5.000kHz
RBW 100Hz   VBW 100Hz   SWP 2.0sec

FIGURE 13 1ˢᵗ L.O. MULTI. (×2, ×3 & ×3) TO 515 MHZ

DOUBLER

SMA/BNC
57.2 MHZ OUT (-12dBm)

J18
3dB ATTEN
28.64 MHZ IN FROM OSC. ~3dBm
SMA/BNC

+15   1μF TANT.   1000 PF
2N5179   150Ω
T1   6.8 kΩ   1000pf
20Ω   2N5179   150Ω
1000 PF

+15 vdc   +15

+15   1μF TANT.   F.B.   50Ω   56 PF
T2   2PF   7-25 PF   7-15 PF   T3

1.2kΩ   10k   2N2222
10k   330Ω
1000 PF   0dBm

L1   47 kΩ   +15   220Ω   F.B.
1000 PF   100Ω   MRF 901   7.5 PF
5 PF   2.4 kΩ

171.86 MHZ BPF

X3

+15   +15 vdc
171.8 OUT 0dBm
0.085" 50Ω SEMIRIGID

171.8 IN 0dBm
0.085" 50Ω Semirigid   +15 vdc   +15
1μF   +15
1000pf   560Ω   1000pf
DISC.   MAR6   DISC.

0.085 50Ω SEMIRIGID
515.592 MHZ BPF   -5dBm

X3   AMP

1μF   +15   +15
270Ω
1000 PF   1kΩ   F.B.   1000 PF
DISC.   MAR-3   CHIP   SMA/BNC
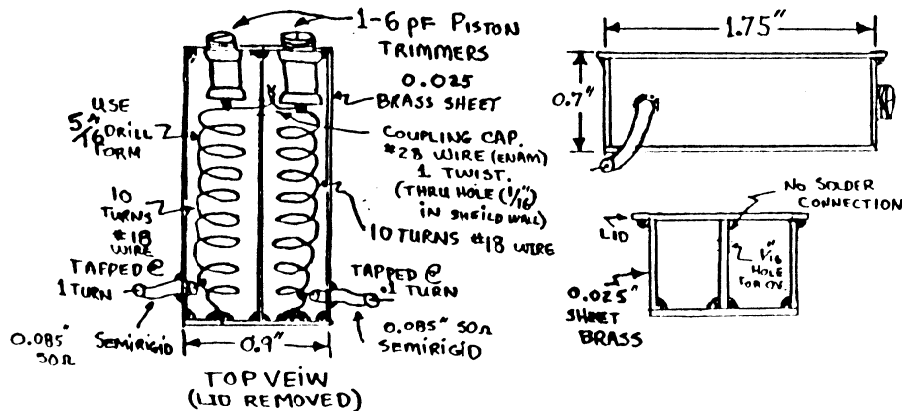
~7 dBM 515.592 MHZ OUT TO X3 MULTI.

IL1 — 3 TURNS, #28, 0.15" DIA.

T1 — 12 TURNS PRI.
10 TURNS SEC. CENTER TAPPED.
#28 WIRE, T50-2 CORE

T2 — 3 TURNS PRI.
12 TURNS SEC.
#28 T30-10 CORE

T3 — 15 TURNS PRI.
2 TURNS SEC.
#28 T30-10 CORE.
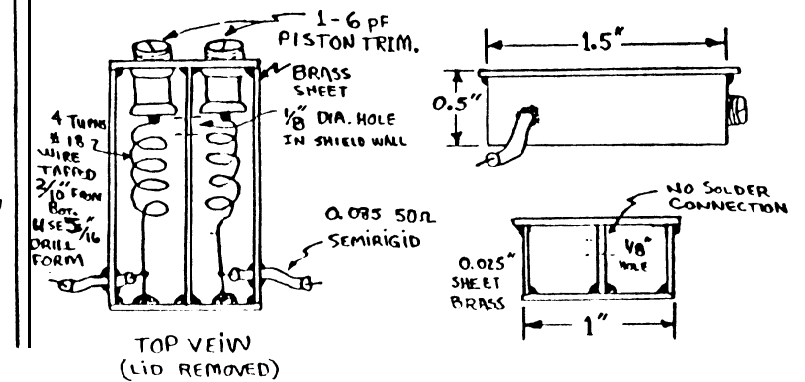
---

171 BPF DETAIL

1-6 pF PISTON TRIMMERS
0.025 BRASS SHEET
COUPLING CAP. #28 WIRE (ENAM) 1 TWIST. (THRU HOLE (1/16) IN SHIELD WALL)
10 TURNS #18 WIRE

USE 5/16 DRILL FORM
10 TURNS #18 WIRE
TAPPED @ 1 TURN
TAPPED @ 1 TURN

0.085" 50Ω Semirigid   0.9"   0.085" 50Ω Semirigid

TOP VEIW (LID REMOVED)

1.75"   0.7"

NO SOLDER CONNECTION
LID
1/16 HOLE FOR OV.
0.025" SHEET BRASS

515 BPF DETAIL

1-6 pF PISTON TRIM.
BRASS SHEET
1/8" DIA. HOLE IN SHIELD WALL

4 TURNS #18 WIRE TAPPED 2/10 FROM BOT. USE 5/16 DRILL FORM

0.085 50Ω SEMIRIGID

TOP VEIW (LID REMOVED)

1.5"   0.5"

NO SOLDER CONNECTION
0.025" SHEET BRASS   1/8" WIRE
1"

FIGURE 15. 1st L.O. 515 to 1546 ARTWORK SHOWN IN NEGATIVE.

x3 mul

in

SCALE 1:1

in ▫

out ▫
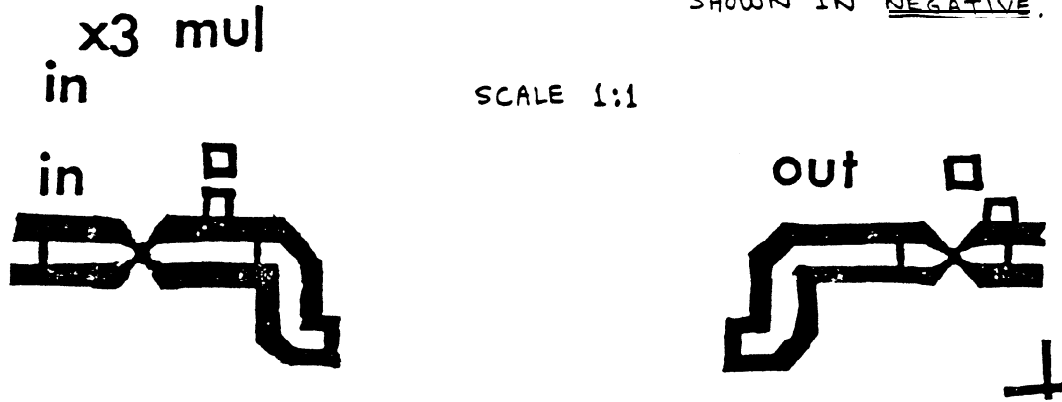
FIGURE 16. LAYOUT OF 1st L.O. 515 TO 1546 x3 MULT.

x3 mul

in

in

+15

1μF TANT.

450Ω

1000pF

1μF TANT.

TO +15

270Ω

MAR 4

out

1/16" G10 BOARD

SMA ~7dBm

1000pF

MAR 8

1pF

1000pF

1.2pF

SMA ~7dBM

X3 SECTION

INTERDIGITAL BPF (@ 1546 MHz)

AMP

FOIL TAPE OVER EDGE SOLDER BOTH SIDES

NOTE: SHIELD BOXES WERE PLACED OVER BOTH THE X3 AND AMP SECTIONS WITH F.T. CAP's FOR the +15.

● " INDICATES SOLID WIRE CONNECTION TO BACK PLANE
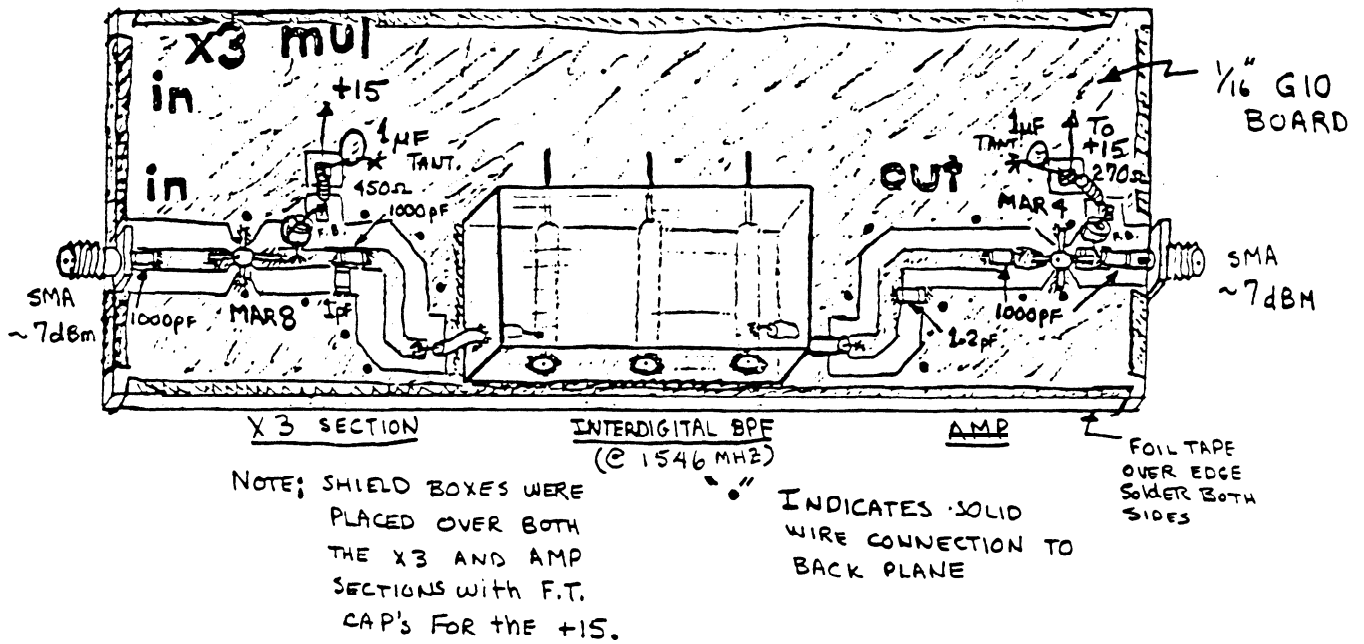
1546 MHz BPF DETAIL (SEE ARRL 1988 HANDBOOK)

0.141" DIA. 50Ω SEMIRIGID COAX RG 402U

1.05"

0.25"

0.085" DIA. 50Ω SEMIRIGID RG 405U

0.025" SHEET BRASS

1.17"

A -

0.144" DIA

2"

0.25"

0.7"   0.7"

0.5"

0.035" DIA

0.25"

FIGURE 17A
28.644 XTAL OSC. W/BUFFER

T1   15/1 TURNS   T-37-2 CORE

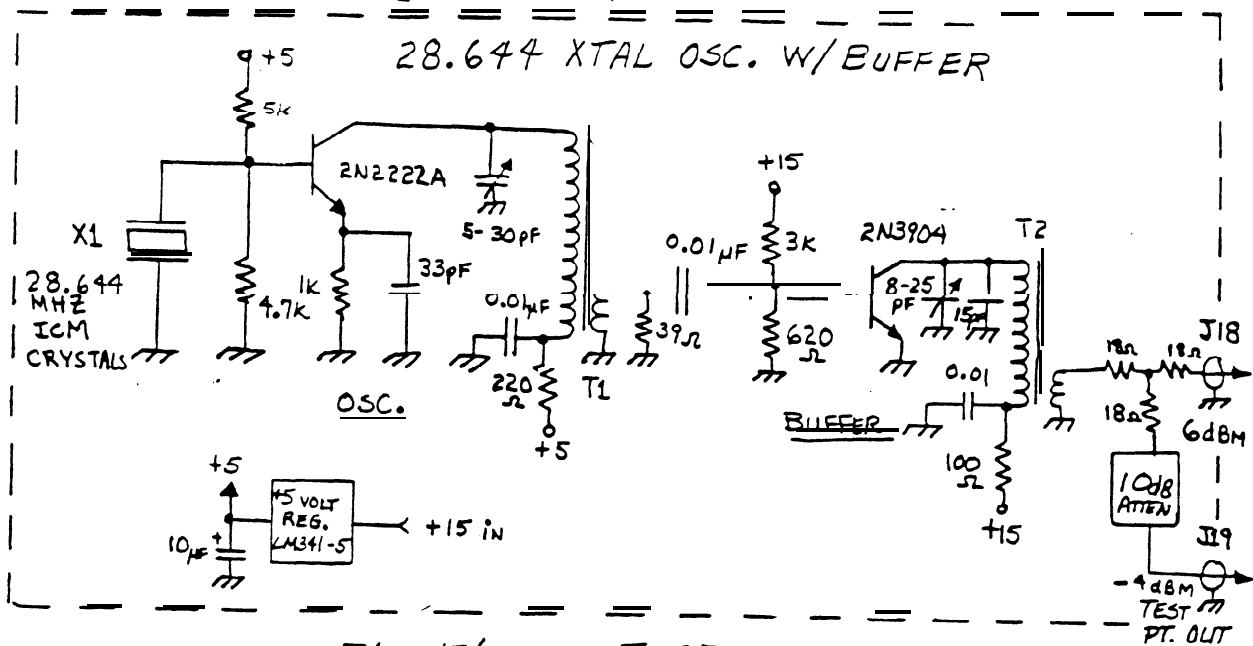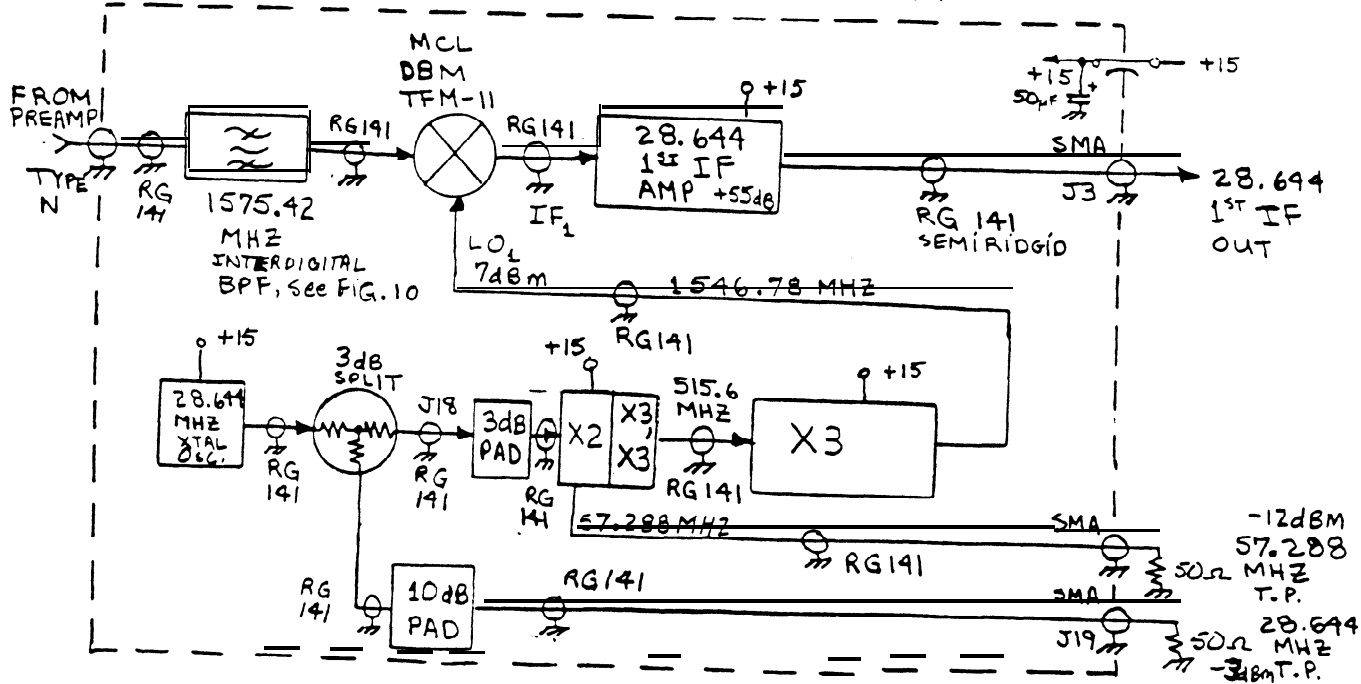T2   15/2 TURNS   T-37-2 CORE
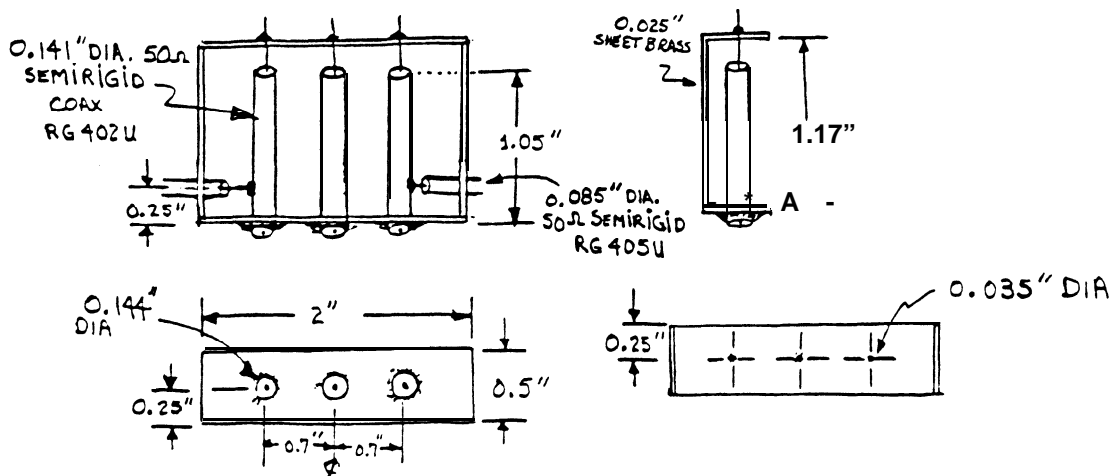
FIGURE 17B
XTAL DOWNCONVERTER
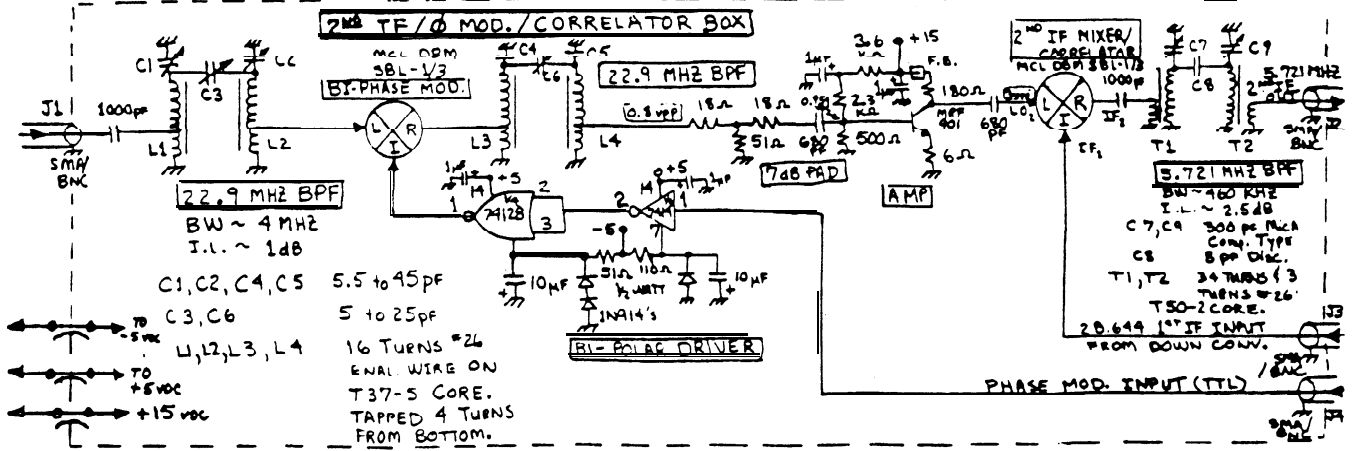
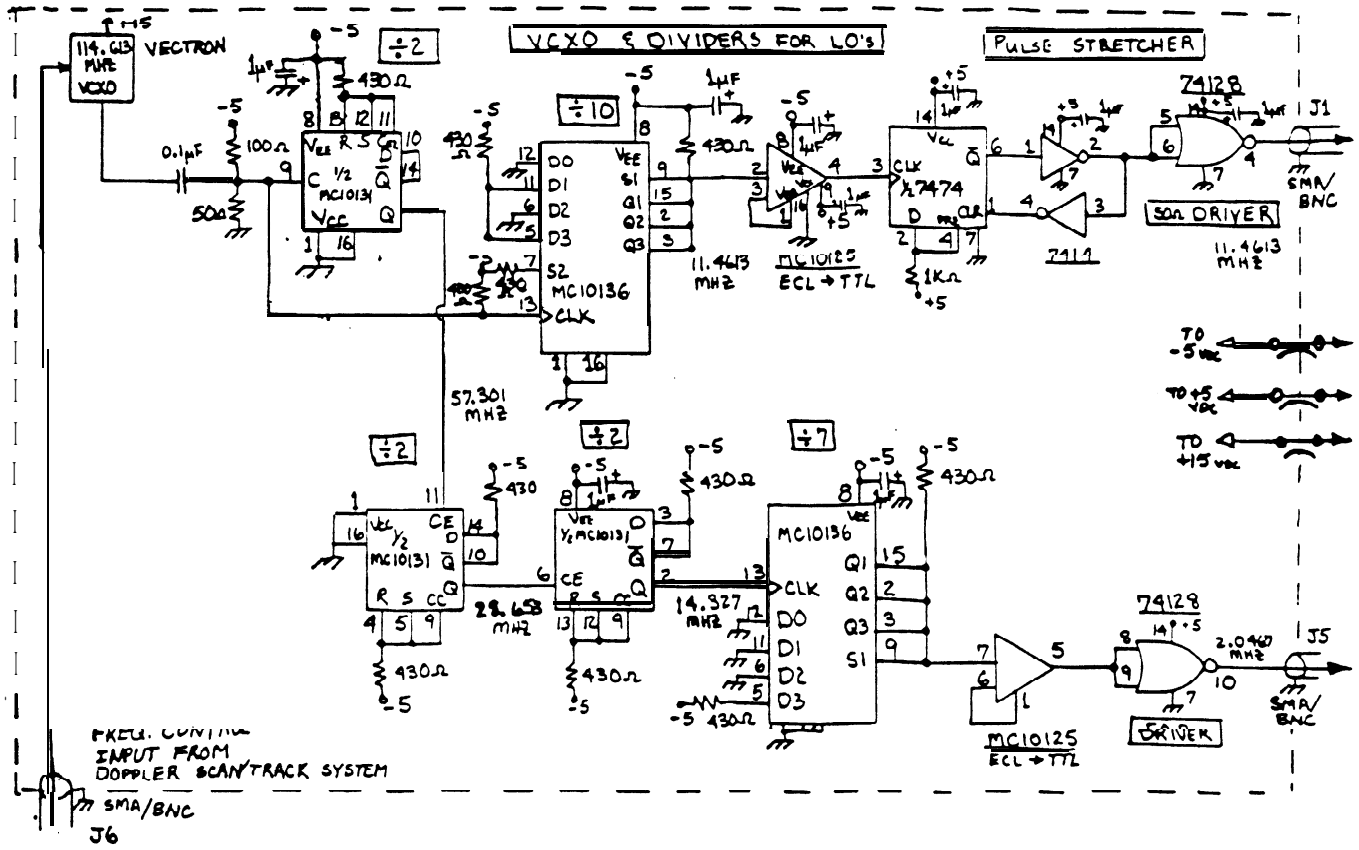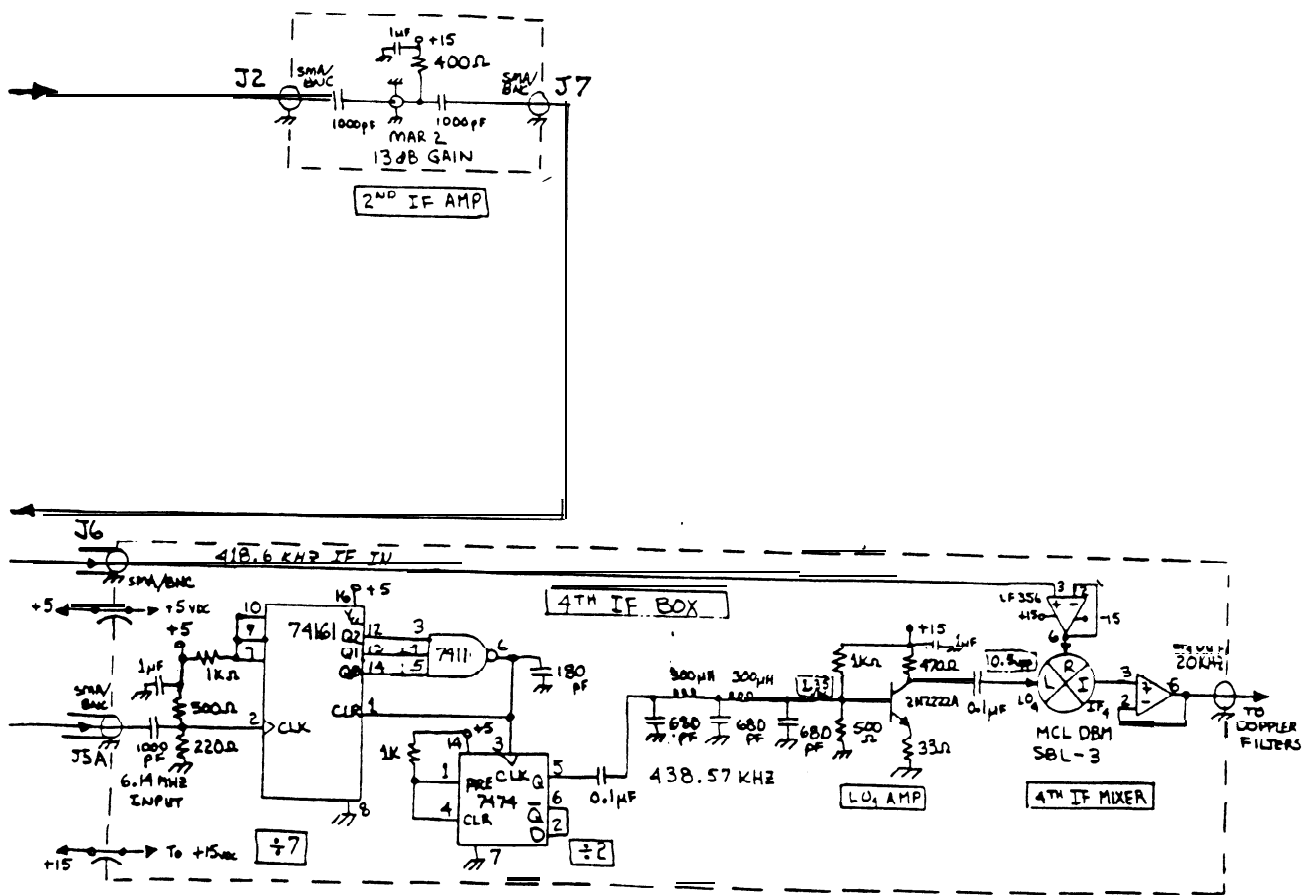# FIGURE 18
2ND, 3RD, 4TH LO's & IF's CIRCUIT(s)
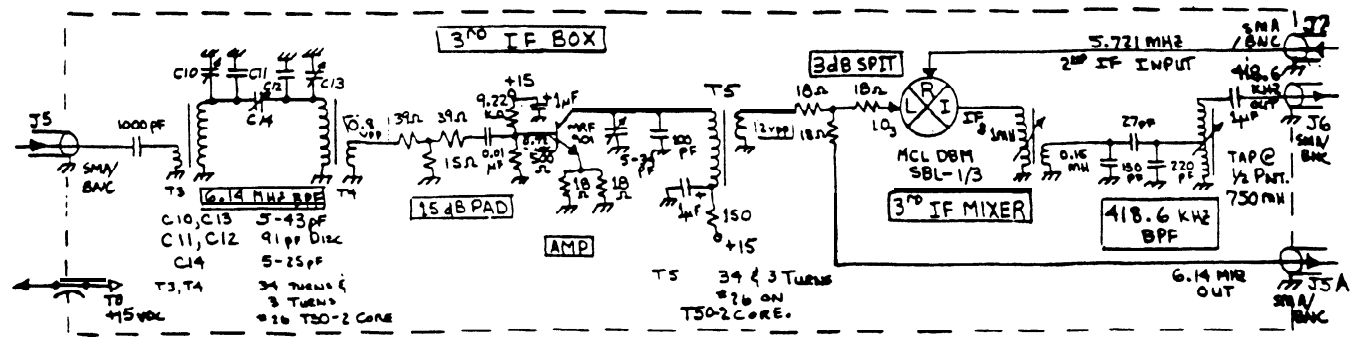
FIGURE 18 CONT.

FIGURE 19

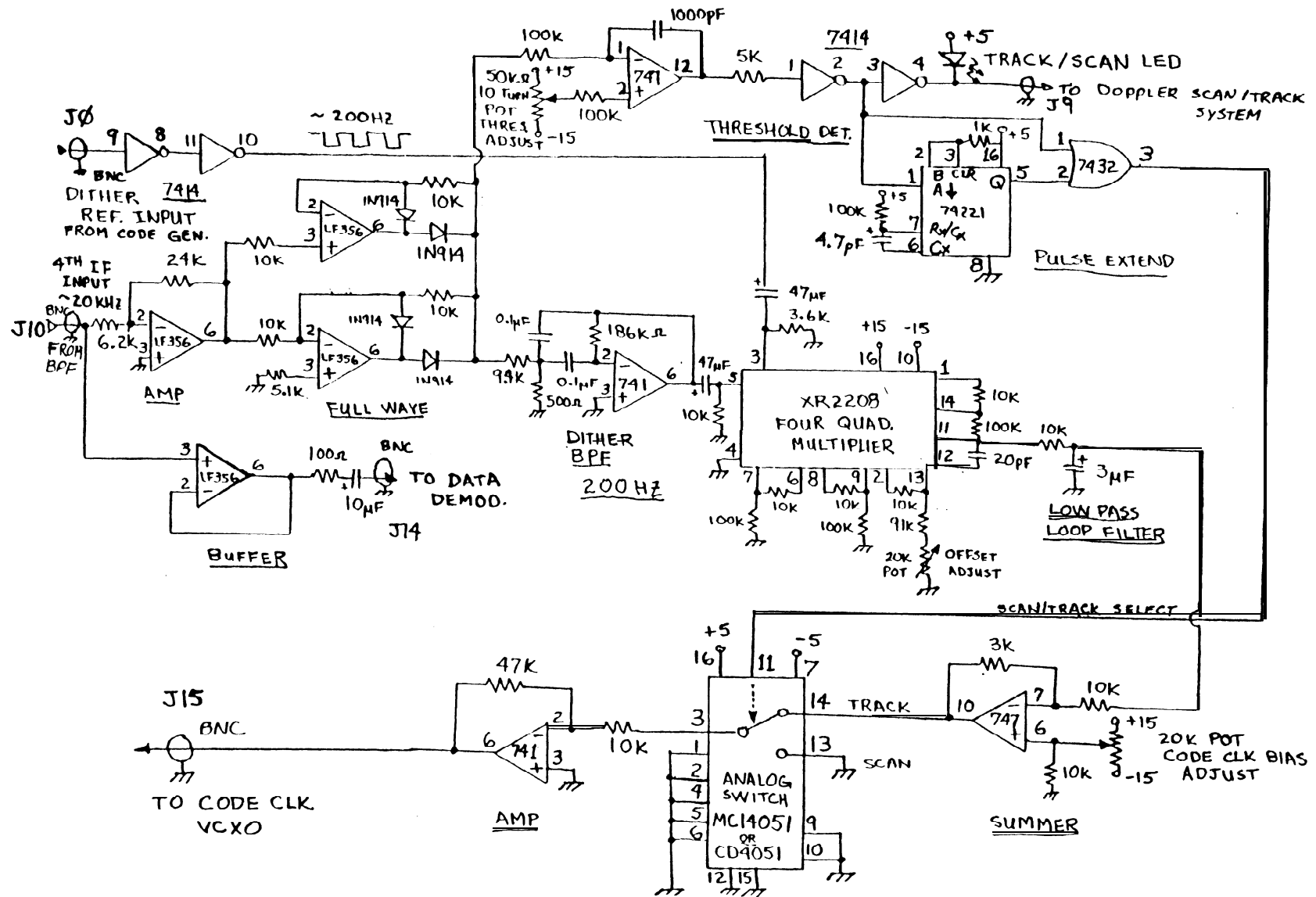## BLOCK DIAGRAM C/A CODE SCAN/TRACK SYSTEM

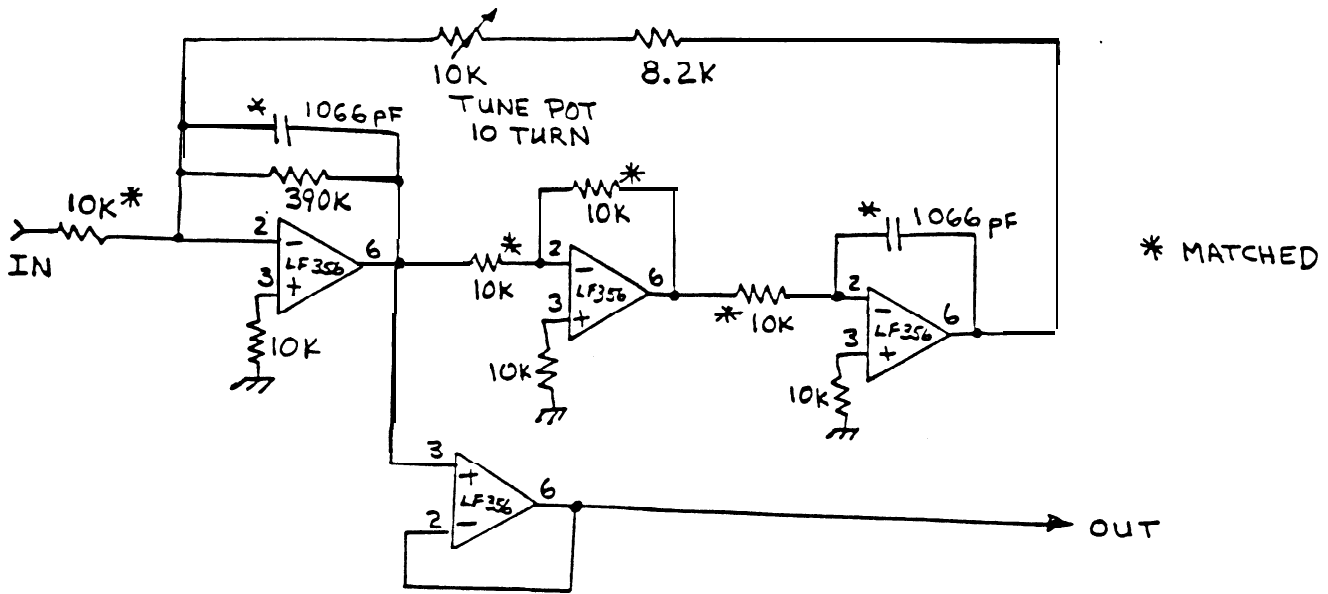* OPEN LOOP WAVEFORMS
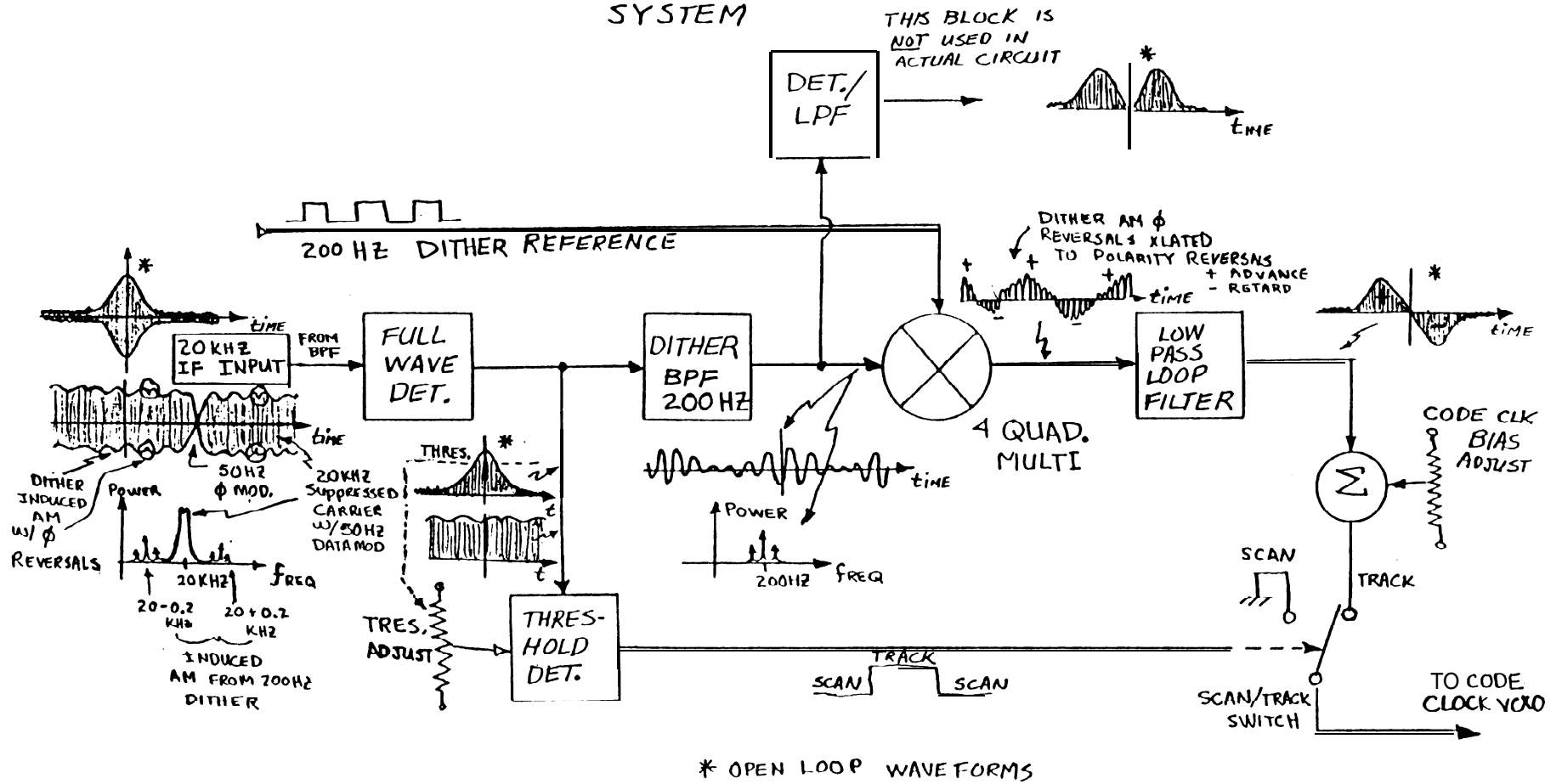
FIGURE 20.
C/A CODE SCAN/TRACK CIRCUIT

FIGURE 21

ACTIVE 20KHZ BPF - SEE OP AMP
COOKBOOK
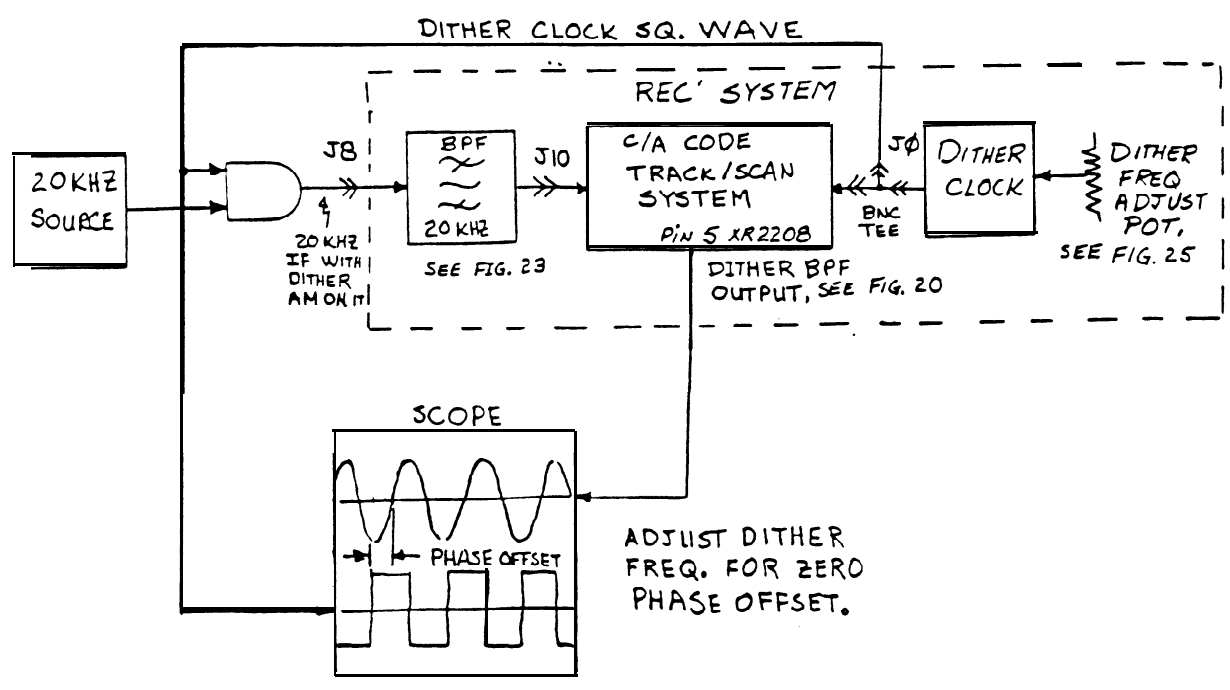

FIGURE 22

DITHER CLOCK TUNING SETUP

FIGURE 23
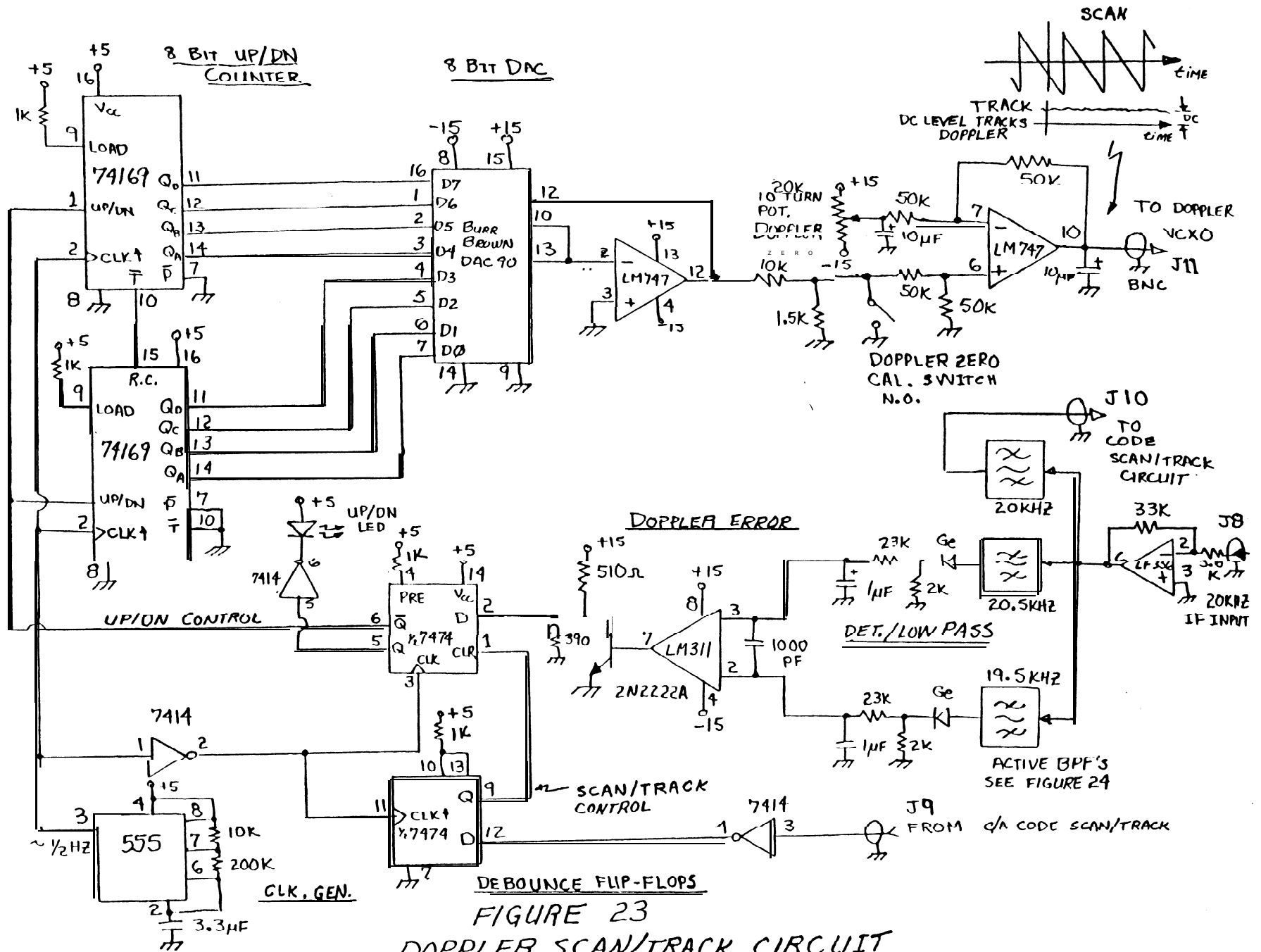DOPPLER SCAN/TRACK CIRCUIT

FIGURE 25

C/A CODE GENERATOR WITH DITHER CODE
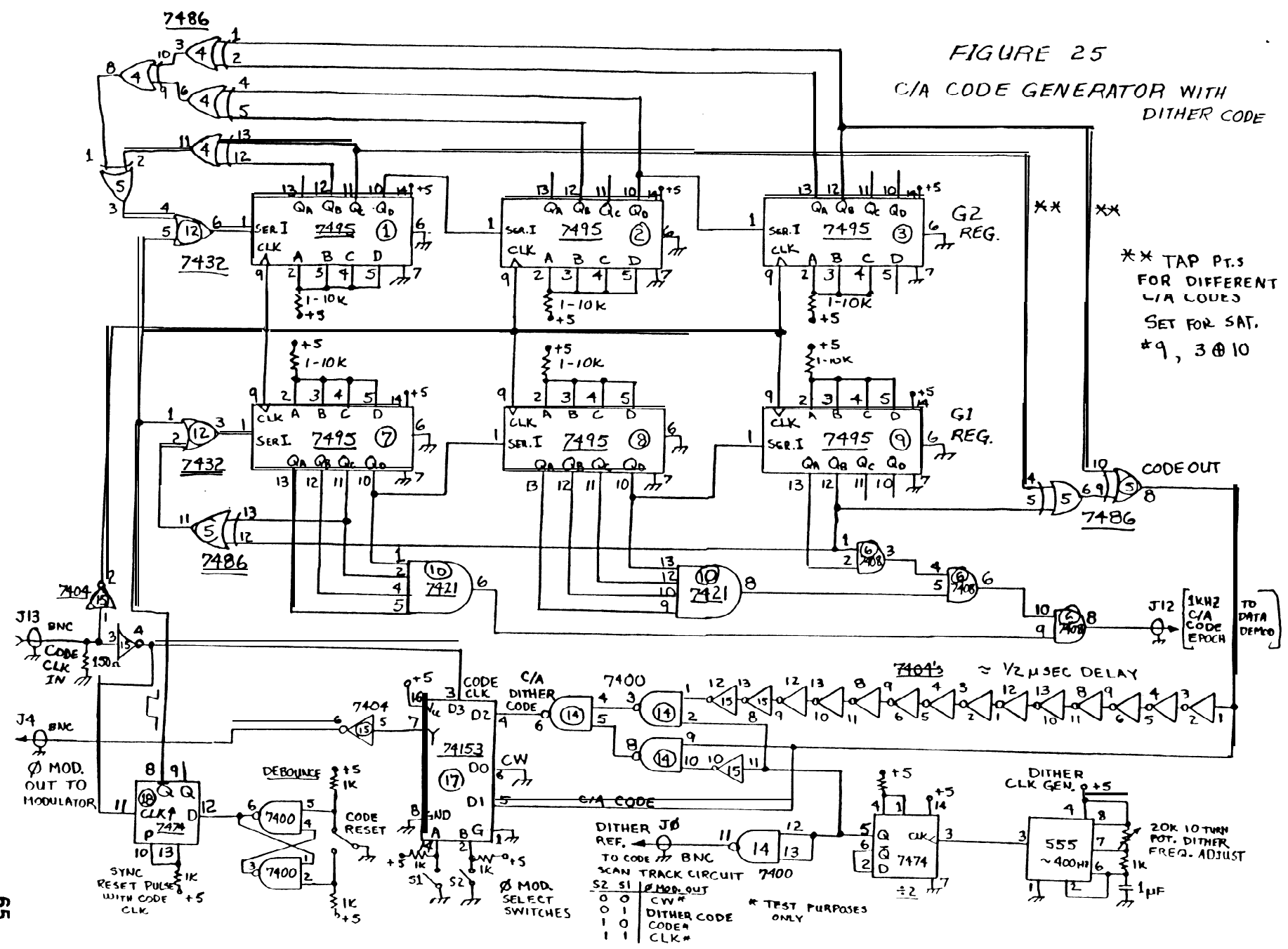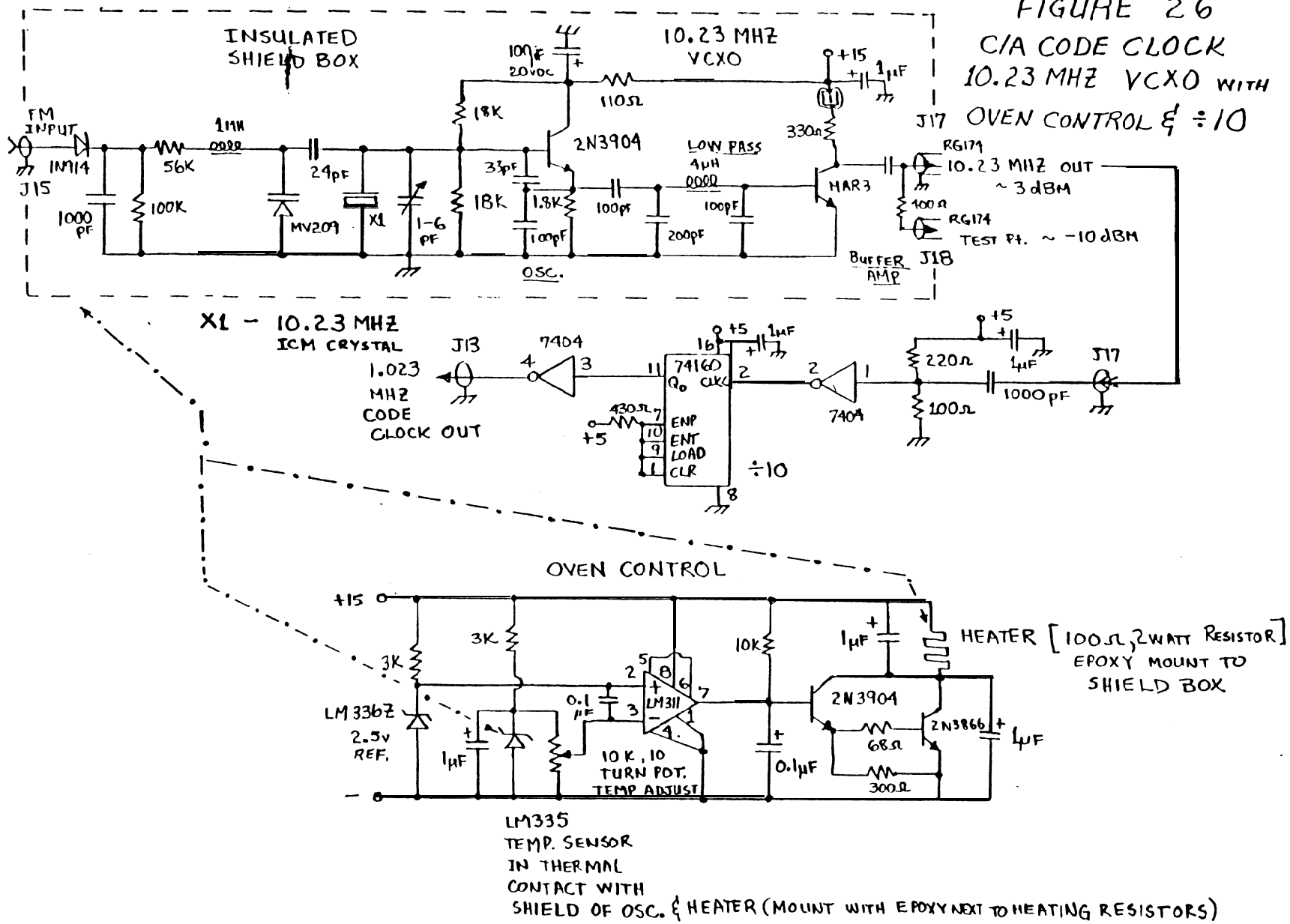
FIGURE 26
C/A CODE CLOCK
10.23 MHz VCXO WITH
OVEN CONTROL & ÷10

INSULATED SHIELD BOX

10.23 MHz VCXO

FM INPUT
J15

1N914

56K
100K
1000 pF

1mH 0000

24 pF

MV209

X1

1-6 pF

18K
18K
1.8K
33 pF
100 pF

100 µF 20 VDC

110Ω

2N3904

LOW PASS 4µH 0000

100 pF
200 pF

100 pF

MAR3

330Ω

+15
1µF

RG174
10.23 MHz OUT ~3 dBM

100Ω

RG174
TEST Pt. ~ -10 dBM

BUFFER AMP   J18

OSC.

X1 - 10.23 MHz
ICM CRYSTAL

J13
1.023 MHz
CODE
CLOCK OUT

7404
4 3

11 74160
Qo CLK
ENP
ENT
LOAD
CLR
8

+5 1µF

430Ω
+5

÷10

2 1
7404

220Ω
100Ω

+5
1µF
1000 pF

J17

OVEN CONTROL

+15

3K
3K

LM336Z
2.5v REF.

1µF

0.1 µF
3 LM311
2 5 8
6
7
4

10K, 10
TURN POT.
TEMP ADJUST

10K

0.1µF

1µF

2N3904
68Ω
2N3866
300Ω

+
4µF

+
1µF

HEATER [100Ω, 2 WATT RESISTOR]
EPOXY MOUNT TO
SHIELD BOX

LM335
TEMP. SENSOR
IN THERMAL
CONTACT WITH
SHIELD OF OSC. & HEATER (MOUNT WITH EPOXY NEXT TO HEATING RESISTORS)

FIGURE 27
DATA DEMODULATOR BLOCK DIAGRAM

Eliminate

20KHZ CARRIER INPUT WITH 50HZ BPSK → PLL → ABSOLUTE VALUE → SCHMITT → PULSE EXTEND → ÷2 → DATA OUT
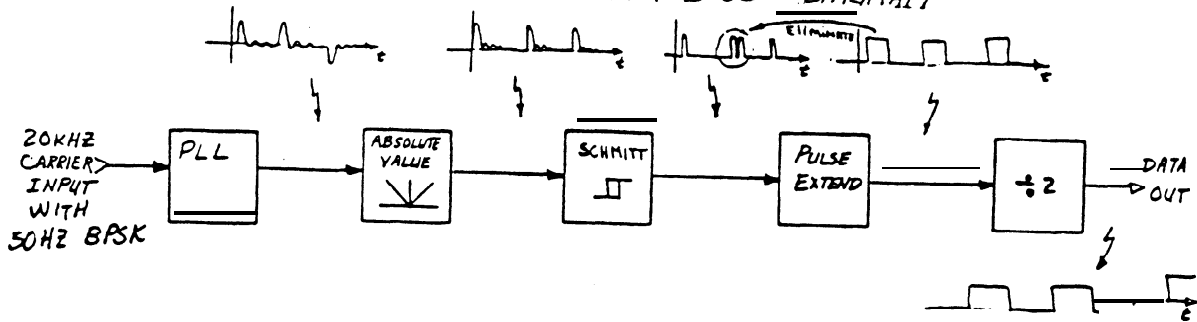
FIGURE 28
DATA DEMODULATOR / DATA CLOCK

LIMITER
20KHZ IF IN
J14
J15
560Ω
IF OUT TEST PT.
500K
PLL
CD4046
VCO
LOOP FILTER
5K,10 TURN POT. VCO ADJUST
10K
0.1µF
1000 PF

FULL WAVE
-1.2v
10K
741
10K
1N914
741
1N914

24K
10K
741
AMP
30K
7414

SQUARE UP
R.C.
74221
PULSE EXTEND
10K
1K

J15 50HZ DATA OUT BNC
7414
9 3
Q
CLK
7474
÷2

÷2
J16 7414
50HZ DATA CLK.
Q
CLK
7474
÷10
CLK
74160
CLK
ENP
ENT
LOAD

J12
1KHZ C/A CODE EPOCH FROM CODE GEN.
BNC

FIGURE 29
ELEVATION PLOT SATELITE VEH. #9
FOR NOV. 23 1989 LAT.=34°6' LONG=-119°6'

DEGREES ABOVE HORIZON
90°
80°
70°
60°
50°
40°
30°
20°
10°

0100 0200 0300 0400 0500 0600 0700 0800 0900 1000 1100 1200 1300 1400 1500
PACIFIC STAND. TIME
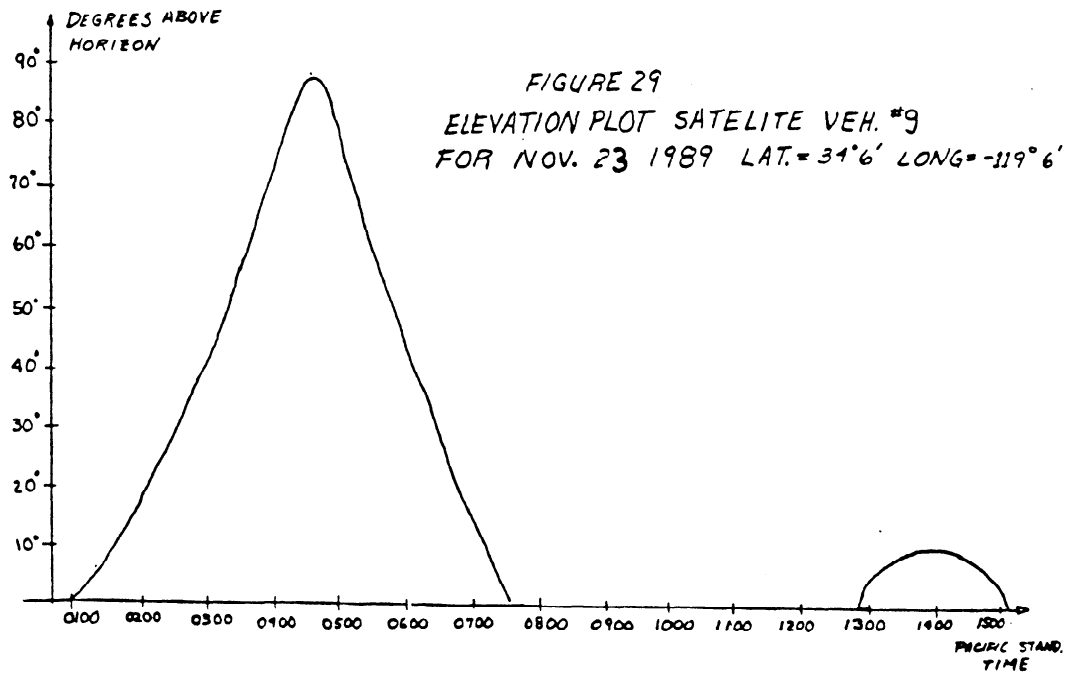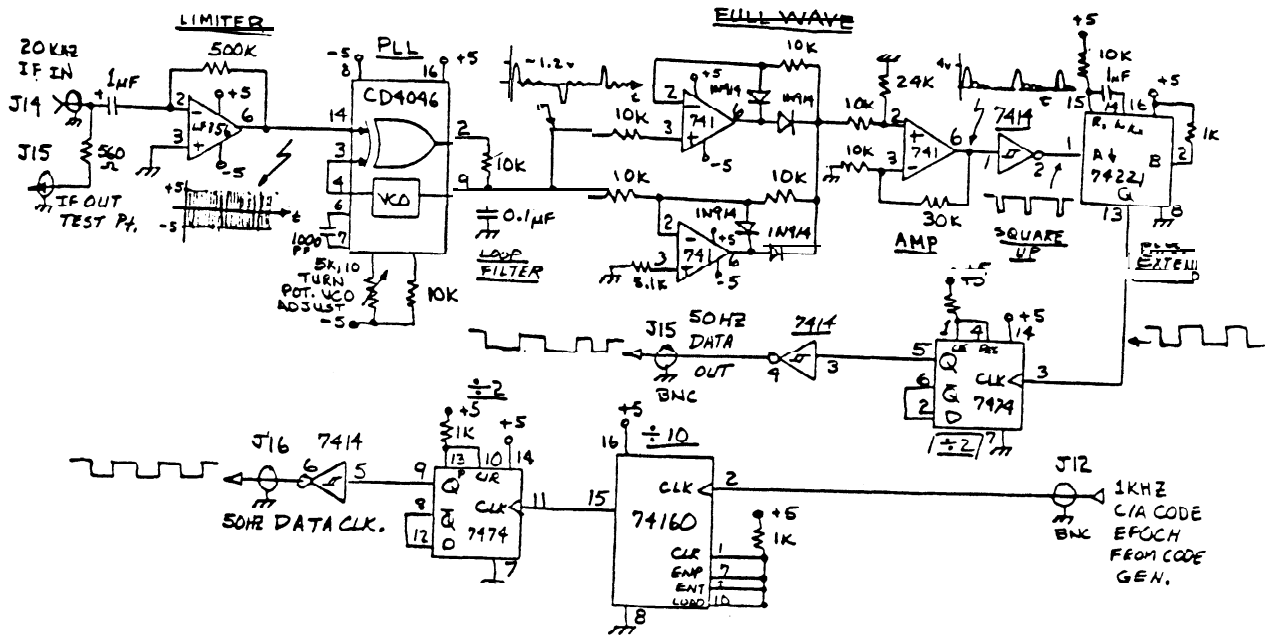
67

FIGURE 30

DETECTED IF & DOPPLER VOLTAGES FOR NOV. 23, 1989
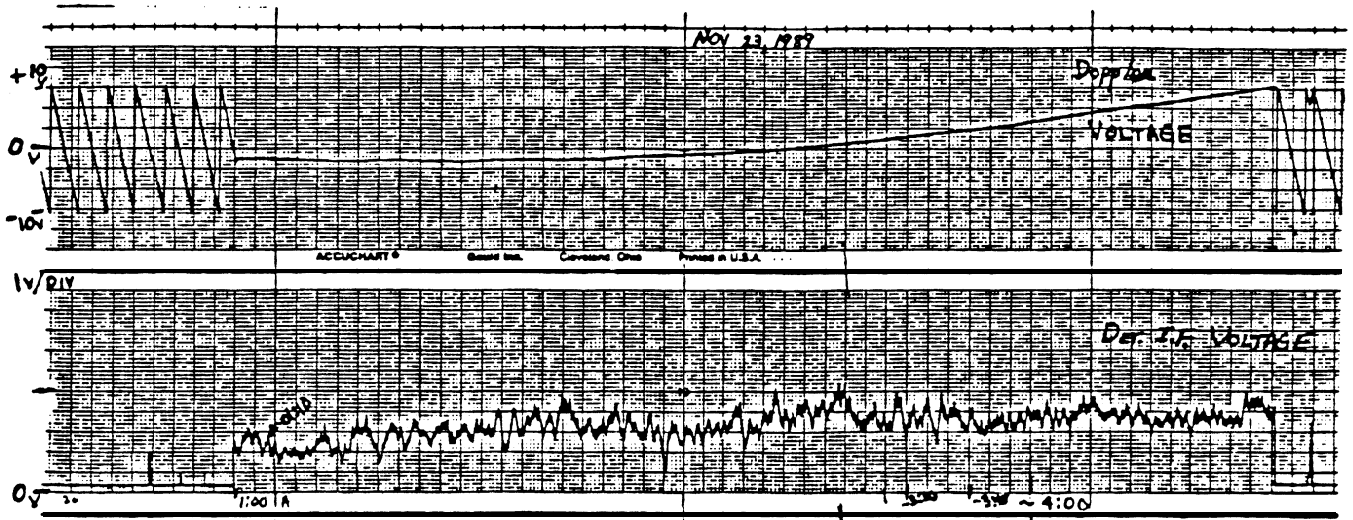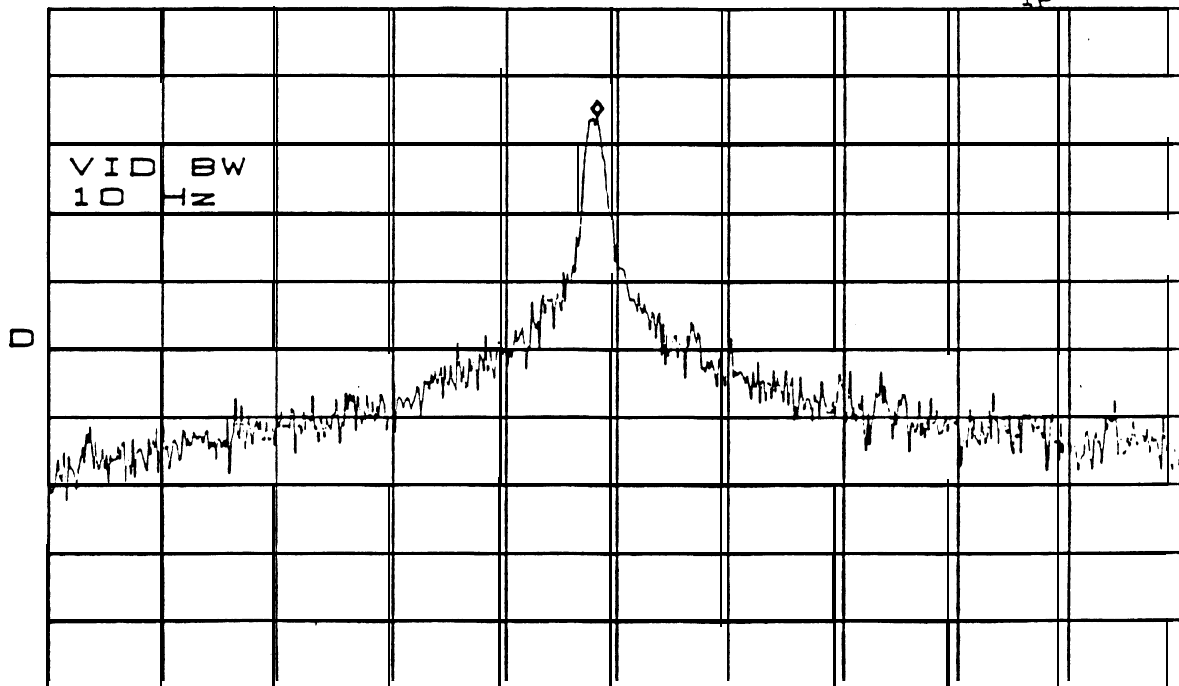### SAT. VECH. #9

FIGURE 31

20 KHZ IF SPECTRUM FROM
SAT. VECH. #9, NOV 23, 1989; ~1400 P.S.T.
TAKEN AT J14 POINT - SEE FIG. 20

＊ATTEN 20dB   MKR −5.67dBm Nov 23, '89
RL 10.0dBm   10dB/   19.82kHz SAT. 20kHz IF

CENTER 20.00kHz   SPAN 10.00kHz
RBW 100Hz   ＊VBW 10Hz   SWP 30sec

FIGURE 32
SAT. VECH. #9 DATA, NOV 23, 1989
(~0345 PST)

GPSD2F Bit Count	PREAMBLE	FRAME I.D.	FRAME I.D.
			1 6
13	10001011 11000000001111111101000	01111110011000010000 0111110000	
73	100000001101000100000001101011	100110011110001100011011100000	
133	001111100011010001001110011000	010011001100111000100101010101	
193	110100101100010011111111011101	111101001010000000100101111101	
253	111111110000000010111001110101	010011010111000101010100011100	
	PREAMBLE	FRAME I.D.	
			2 5
313	10001011 11000000001111111101000	011111100110000110001010011000	
373	000010111111100000101100101100	000011101001001000111111111100	
433	010110000100110101000011101101	000001110001110111111000110111	
493	100010001111111100111011010011	111100000101010001011110000110	
553	000011010000000100010101000100	101000000011001010101001101000	
	PREAMBLE	FRAME ID.	
			3 4
613	10001011 11000000001111111101000	011111100110001000001110100100	
673	111111110111111111000011101100	011001101001111111100100001001	
733	000000000011110111010010001100	010110110110011111010000010101	
793	110110001101000111010100011001	001010011011000110000001111001	
853	000000000100011100001100000100	000010111111001000111111010100	
			4 3
913	10001011 11000000001111111101000	011111100110001010001100000	
973	011101100100000001918000011011	110111111101111111101111111101100	
1033	001000000010000000100000010011	110111111101111111101111111181188	
1093	001000000001000000001000000010011	110111111101111111101111111101100	
1153	001000000018000001188888818811	110111111101111101018111811188	
			5 2
1213	10001011 11000000001111111101000	011111100110001100~10010000	
1273	010000001010101010101010101100	101010101010101010101010111100	
1333	101010101010101010101010111100	101010101010101010101010111100	
1393	101010101010101010101818111188	101010101010101010101010111100	
1453	101010101010101010101010111100	101010101010101010101010J11100	
			1 6
1513	10001011 11000000001111111101000	011111100110001110001011011000	
1573	100000001101000100000001101011	100110011110001100011011100000	
1633	001111100011010001001110011000	010011001100111000100101010101	
1693	110100101100010011111111011101	111101001010000000100101111101	
1753	111111110000000010111001110101	010011010111000101010100011100	
			2 5
1813	10001011 11000000001111111101000	011111100110010000001001111000	
1873	000010111111100000101100101100	000011101001001000111111111100	
1933	010110000100110101000011101101	000001110001110111111000110111	
1993	100010001111111100111011010011	111100000101010001011118888118	
2053	000011010000000100010101000100	101000000011001010101001101000	
			3 4
2113	10001011 110000000011111110+000	011111100110010010011111110000	
2173	111111110111111111000011101100	011001101001111111100100001001	
2233	000000000011110111010010001100	010110110110011111010000010101	
2293	110110001101000111010100011001	001010011011000110000001111001	
2353	000000000100011100001188888188	000010111111001000111111010100	
			4 3
2413	10001011 11000000001111111101000	011111100110010100010001001100	
2473	011110000100100000001001110000	111111100000000001001100010100	
2533	111101101111111100000010001110	111111111111111110011010011001	
2593	000000000000000000000000010101	111000101111011111111011101001	
2653	111110101110110111111110001100	000001101010101010101000010000	
			s 2
2713	10001011 11000000001111111101000	011111100110010110010111000100	
2773	010000001010101010101010101100	101010101010101010101010111100	
2833	101010101010101010101010111100	101010101010101010101010111100	
2893	101010101010101010101010111100	101010101010101010101010111100	
2953	101010101010101010101010111100	101010101010101010101010111100	

TLM WORD

SOLVED FOR BITS TO
PRESERVE PARITY CHECK WITH
TWO TRAILING ZEROS

PARITY

MSB

LSB

| PREAMBLE
1 0 0 0 1 0 1 1 | TLM MESSAGE | | | | 0 | 0 |

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

SYNCHRONIZATION FLAG (FOR SV CONFIG 000) OR
ANTI-SPOOF FLAG (FOR SV CONFIG 001)

MOMENTUM FLAG (FOR SV CONFIG 000) OR
"ALERT" FLAG (FOR SV CONFIG 001)

PARITY

MSB

LSB

| TOW-COUNT MESSAGE
(Truncated) | | | SUB-
FRAME
ID | | | | 0 | 0 |

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
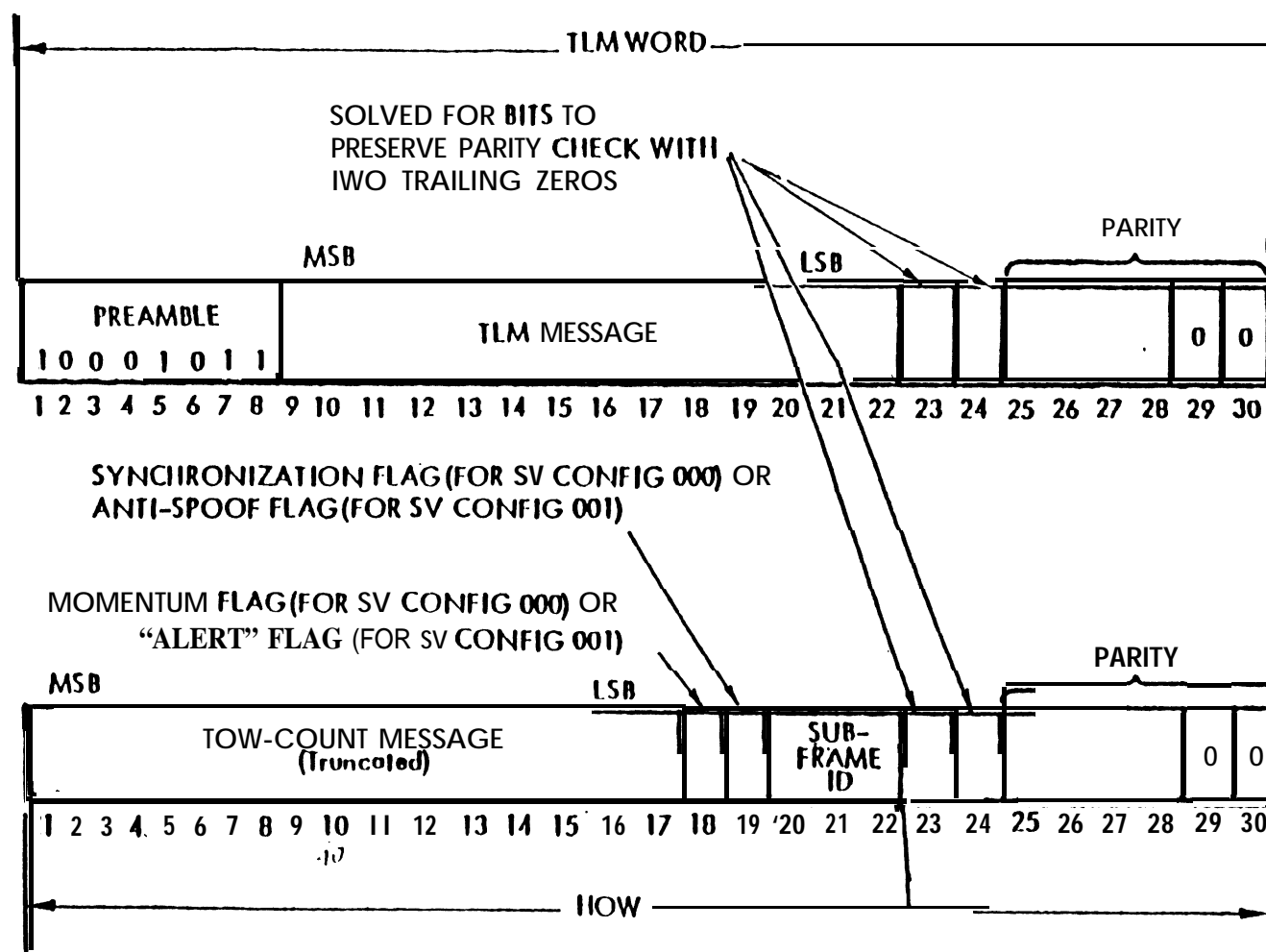
HOW

Figure 33.   TLM and HOW Formats
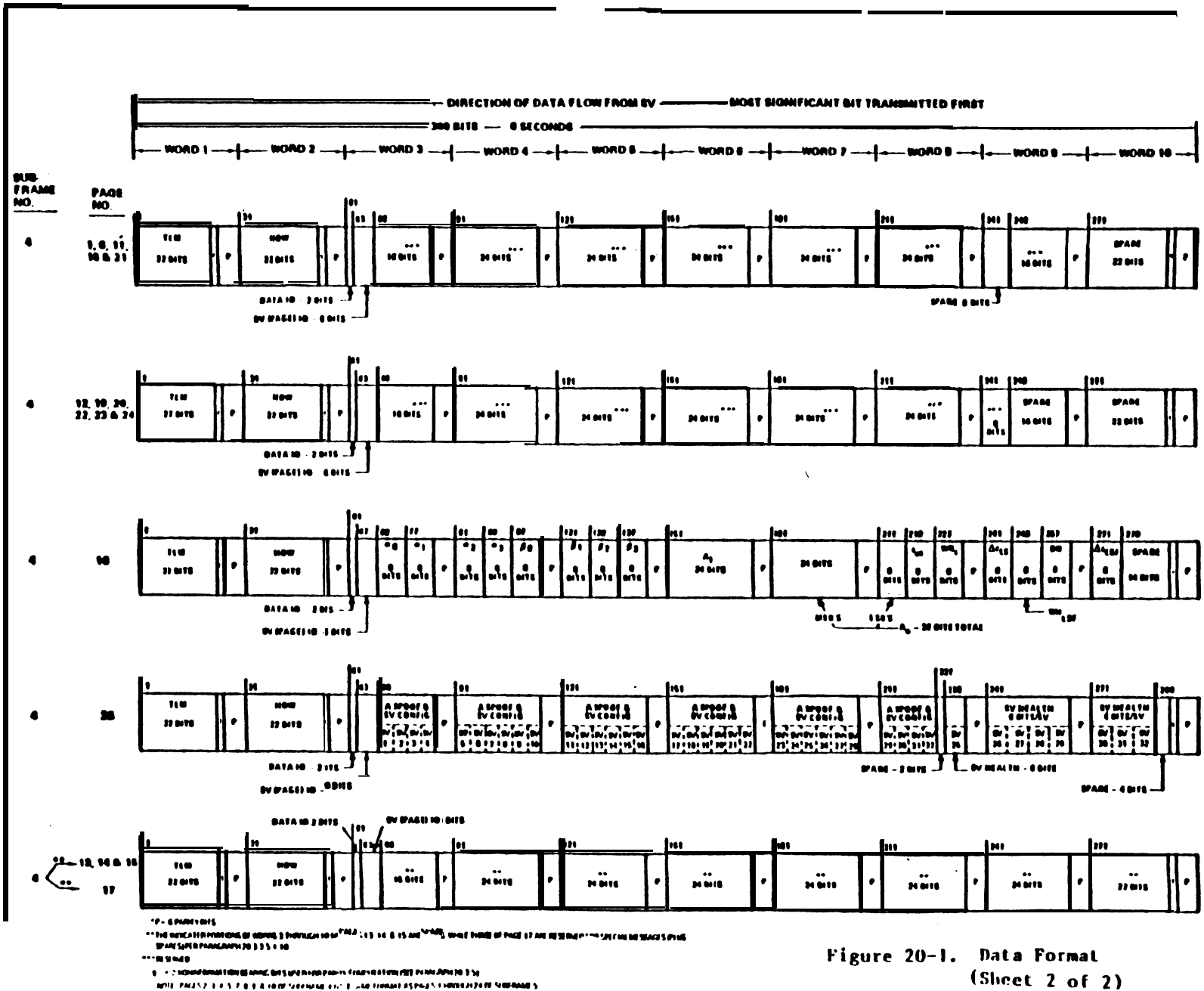
FROM ICD-GPS-200

Figure 20-1. Data Format
(Sheet 2 of 2)

FIGURE 34 A
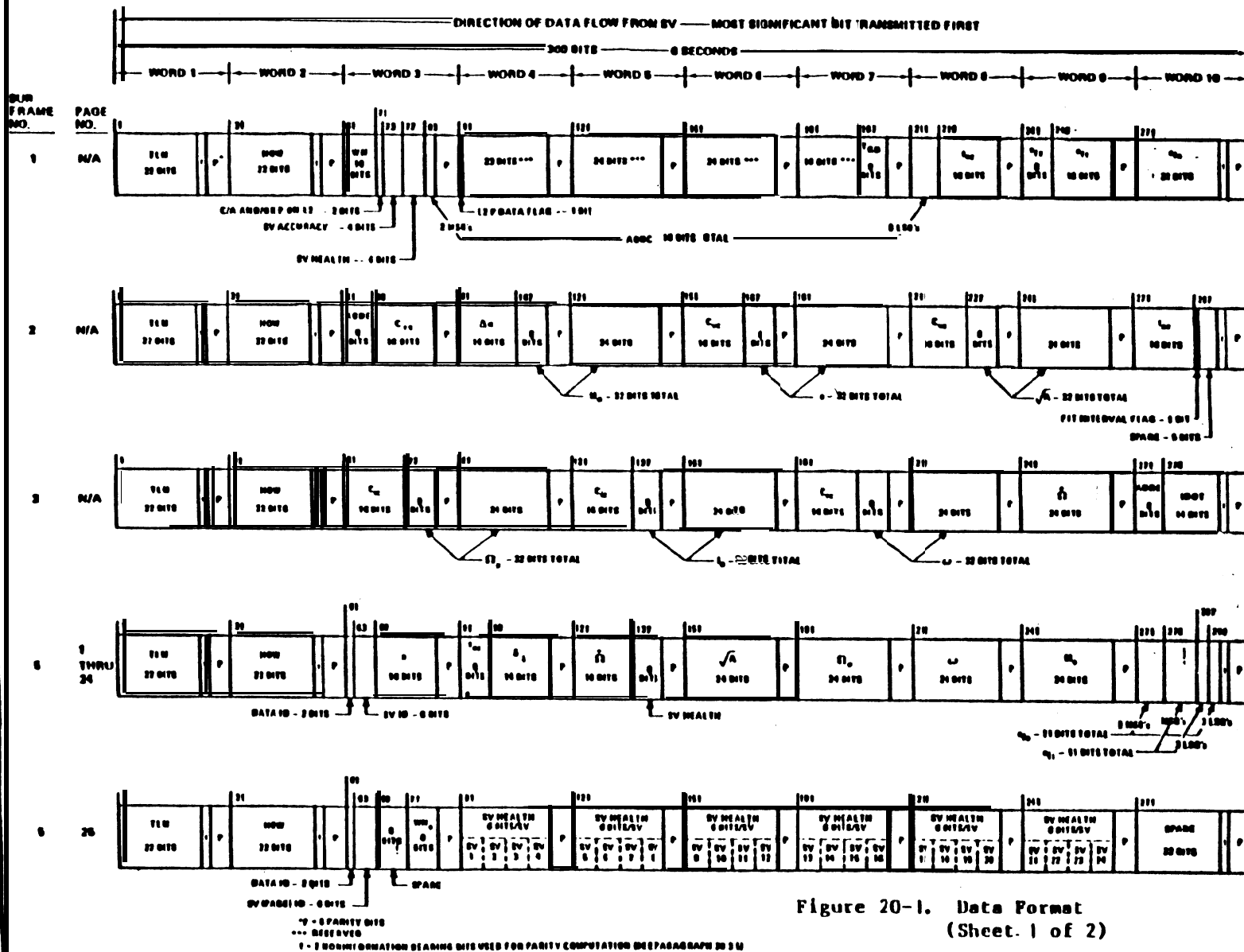DATA FRAME CONTENT CONT.
FROM ICD-GPS-200

Figure 20-1. Data Format
(Sheet. 1 of 2)

FIGURE 34B
DATA FRAME CONTENT

FROM ICD-GPS-200