A Zero-IF digitized Despreading Scheme Without PN Code Synchronization Recovery

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Abstract

Zero-IF is a important method to digitize the despreading.In this paper,a fast zero-IF digital despreading scheme without PN code synchronization recovery is given,which is based on performance analysis to chip rate sampling and multiple chip rate sampling in AD convertor.

Keywords: Zero-IF, despreading , chip rate , sampling , synchronization recovery

Introduction

The 3G telecommunication system standard make the broadband CDMA the main tendency. However, we get higher data rate at expence of more complex and expensive transeiver, especially the despreading receiver.

Digitized spreading / despreading is the most significance development. To direct sequence spread spectrum (DSSS) it means AD convertor (ADc),Digital Match Filter(DMF),ASIC and DSP are used. Most digitized despreading schemes are tecnologicially realized based on zero-IF, especially analog zero-IF for its lower complexity. In this scheme AD converting is a process which sample and quantize baseband chip wave stream, and the sampling determines the post circuit and its performance, so accuracy of the sampling is very important.

In digitized despreading schemes two sampling methods are used---chip rate sampling and multiple chip rate sampling. Sampling clock of the former equal to the chip rate,that is to say receiver just sample the chip wave once in a chip period, but the latter sample two or more times. We can use the former method to design a simplest DMF, but with a accurate PN code synchronization recovery unit as an offset. However the latter can provide accurate sampling under any phase difference between local sampling clock and chip stream, this means that we have possibility to abandon the more complex PN code synchronization recovery unit,certainly, scale of the DMF will expand correspondingly.

In this paper, we make analysis to and comparation between the chip rate sampling and the double chip rate sampling method. We find that the latter can provide enough Signal-Noise Rate(SNR) in general utilization. Based on this discovery, we develop a double chip rate sampling digitized despreading scheme without PN code synchronization recovery unit.

1. Zero-IF DSSS receiver

Zero-IF signal can be generated by analogue or digitized method. The latter demand that Adc(s) is(are) applied in IF band, which make system difficult to realize. In main applications the former is adopted.Figure 1 illustrates a typical analogue zero-IF DSSS receiver.

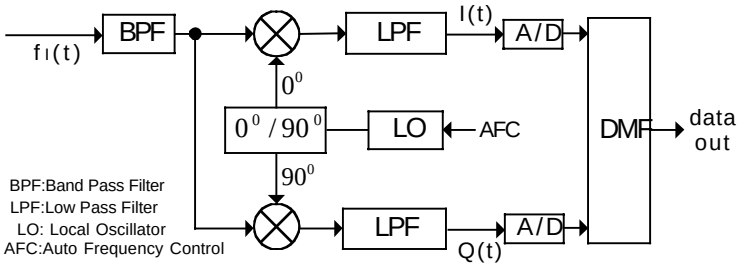

Figure 1 A typical analogue zero-IF DSSS receiver

2. Chip Rate Sampling and Multiple Chip Rate Samp

Bit Error Rate(BER) of a DSSS system in radio channel can be expressed as_

$$P_e = erfc\left(\frac{1}{\sqrt{\frac{K-1}{3N}+\frac{1}{SNR}}}\right) \qquad \_1\_$$

Where $erfc(x)=\frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{-y^2/2}dy$, K is the number of PN codes that arrived at radio channel at same time and N is the length of PN codes(given that all codes' length are same).To make the explanation more clear, we select K =5,20,35 and N =63 and take them into Equation (1),we can get a set of relations between P_e and SNR illustrated in Figure 2.We chose K =20 as a example and easy to find that when $SNR \approx 5dB$ P_e will reach 10^{-3} OM.

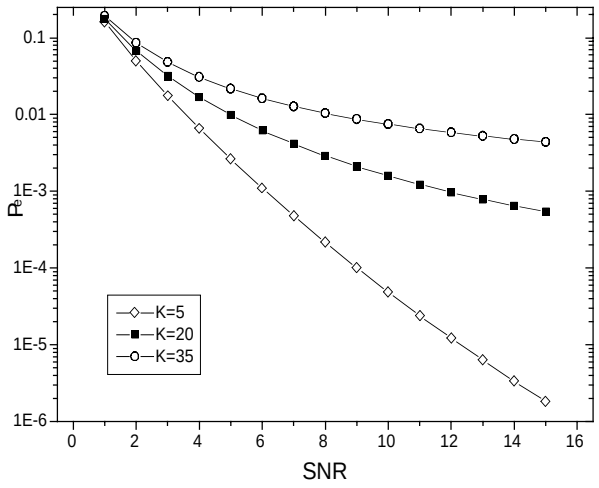

Figure 2 P_e L SNR **curve**

When chip stream is asynchronous to the local PN code clock,a key problem is that how to set the ADc to sample a chip sample as great as SNR.That is so called synchronization.Inserting PN code synchronization recovery unit is a way,but is more hemogeneous.To system illustrated in Figure 1,assuming $d(t)$ =1 or 0 is data bits,if modulation is DPSK,then IF input signal is $f_I(t) = N\sin(\omega_T t + \varphi)d(t)$,where N is amplitude(given as 1 without influence) and ω_T _φ is received carrier frequency and phase deviation respectively.Assuming output of the LO is $\cos(\omega_L t + \theta)$,where ω_L, θ is frequency and phase respectively and other conditions are perfect,then the zero-IF signal passed the LPF is

$$I(t) = [\sin(\omega_T t + \varphi)\cos(\omega_L t + \theta)d(t)] * h(t)$$
$$= [\frac{1}{2}\sin(\Delta\omega t + \Delta\varphi)d(t)] * h(t) \qquad \_2\_$$

and
$$Q(t) = [\sin(\omega_T t + \varphi)\sin(\omega_L t + \theta)d(t)] * h(t)$$
$$= [\frac{1}{2}\cos(\Delta\omega t + \Delta\varphi)d(t)] * h(t) \qquad \_3\_$$

Where $\Delta\omega = \omega_T - \omega_L, \Delta\varphi = \varphi - \theta$,AFC can drive ω_L trend to ω_T ,so $\Delta\omega \approx 0$,thus suppressed the mirror.Assuming $\Delta\varphi$ constant is reasonable, "$*$ " denote convolution, $h(t)$ is the time impulse response of the LPF(we deem it is ideal, i.e.it has rise cosine spectral property).From Equation (2) and (3) we see that $I(t)$

is a function of rise cosine spectral property expressed as Equation (4),so is $Q(t)$ which has same wave as and $\frac{\pi}{2}$ phase diviation to $I(t)$.

$$I(t) = A\frac{\sin(\pi\omega t)}{\pi\omega t}\frac{\cos(\alpha\pi\omega t)}{1-4\alpha^2\omega^2 t^2} \qquad \_4\_$$

Where ω is data rate, α is roll down coefficient and A is amplitude.If $\omega t = T \_ \alpha = 1$,then Equation (4) can be simplified as

$$I = A\frac{\sin(\pi T)}{\pi T}\frac{\cos(\pi T)}{1-4T^2} \qquad \_5\_$$

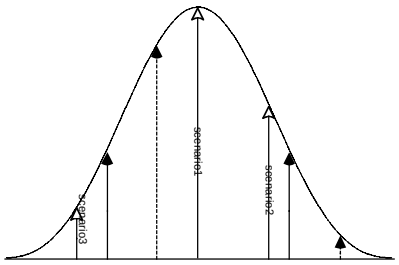

Figure 3 Asynchronous sampling scenarios

We design chip wave can provide maximum SNR which drive P_e to 10^{-4} OM, accroding to Figure 2 the SNR is about 12dB.If chip rate sampling is applied without PN code synchronization recovery unit, just one of three scenarios will appear, which is explained by hollow arrow in Figure 3.

scenario 1: Sampling point just place at the symmetry axis of the chip wave(let this point is $T = 0$).From Equation (5) we can write that

$$I = A\frac{\sin(\pi T)}{\pi T}\frac{\cos(\pi T)}{1-4T^2}\Big|_{T=0} = A \qquad \_6\_$$

In this scenario the DMF can get 12 dB input SNR and output data stream with 10^{-4} OM.

scenario 2: The phase difference between sampling point and the chip wave is less than $\pi/2$,but far higher than zero.The SNR of this sample is less than 12dB,but higher than 5dB,so can make system to get 10^{-3} OM output.

scenario 3: The phase difference between sampling point and the chip wave verge to zero.It is obvious that at this time the receiver can not despread chip stream correctly.

Up to now the key factor can be generalized as where is the bound between the scenario 2 and 3.We notice that I is a monotone function,so this problem equivalent to find the value of T which make I to satisfy $SNR = 5dB$ (let this value of **Error! Not a valid link.** is T_B).We let N_0 denote average noise power,thus the SNR can be defined as

$$SNR = 10\lg\left(I^2 \big/ 2N_0\right) \qquad \_7\_$$

Let $SNR_H = 12dB$, $SNR_L = 5dB$,from Equation (5) (7) we can show that

$$\frac{A^2}{2N_0} = 10^{SNR/10} \qquad \_8\_$$

and $$SNR\Big|_{T=T_B} = SNR_L = 10\lg \frac{A^2\left[\dfrac{\sin(\pi T_B)\cos(\pi T_B)}{\pi T_B(1-4T_B{}^2)}\right]^2}{2N_0} \qquad \_9\_$$

Take_8_ into _9_ we get

$$\frac{\sin(\pi T_B)}{\pi T_B}\frac{\cos(\pi T_B)}{1-4T_B{}^2} = \sqrt{10^{\frac{SNR_L - SNR_H}{10}}} \qquad \_10\_$$

We solve Equation (10) and get the bound:$T_B \approx 0.5358$ .From (5) we know when $T \approx 1$,I=0, i.e.if duration of the chip wave is 2 and phase difference between sampling point and the chip wave is uniform distribution between 0 and 2π,the sampling point must fall into the scope that the maximun and minimum T is +0.5358 and –0.5358 respectively to enable P_e to touch 10^{-3} OM. It is clear to see chip rate sampling without PN code synchronization recovery is very easy to sample incorrectly, the probability is about 1-0.5358 = 46.42%.

If we increase sampling rate to double chip rate,as solid arrow showing in Figure 3,the result will be dramaticly changed.It is in evidence that the higher one of the two samples reach to its minimum just when the two sample equal(showed as solid line solid arrow in Figure 3),in any other scenario there is always a sample of the two higher than the worst minimum(showed as dashed line solid arrow in Figure 3).By the derivation method just as above-mentioned we can know that the worst minimum appears when two sample happen to place at T=+0.5 and T=-0.5 respectively.The conclusion we have got tell us in this worst scenario P_e still can sure 10^{-3} OM.That means error sampling probability can be zero.

3. Fast Zero-IF digitized despreading scheme based on double chip rate sampling

Analysis gave above show we that double chip rate sampling can provide satisfactory result under arbitrary asynchronous phase. It hint the PN code synchronization recovery unit can be omitted and we are able to design a fast despreading sysytem.

We select 32-tap DMF as the basic despreading unit. PN code length is 32 bits. Aimed to realize double chip rate sampling, we introduce a 64-tap serial shift register whose length is double the PN code's. We divide the register into two groups without modification of its connection. The two groups together with a common 32-tap reference register form two 32-tap digital correlators. The concrete division method is the registers with odd serial number from input port form group 1,the even ones group 2.The group 1 store the former of the two samples of one chip wave(i.e.the sample shifting into register advanced) and group 2 the latter.It is obvious that in one of utmost 127 samlping clock periods group 1 and 2 just right store the PN code's two groups samples respcetively, and at least one of the two correlators will output correct correlation peak instantly. If two peaks are outputed at same time, the higher will be reserved and used for demodulation. All mentioned above are illustrated in Figure 4.

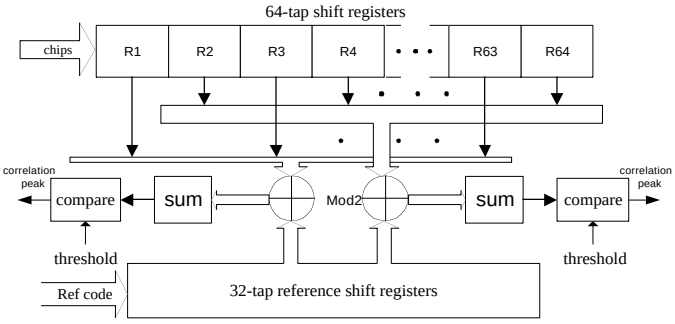

Figure 4 Double chip rate sampling fast zero-IF digitized despreading scheme

We designed and simulated the scheme in a FLEX10K10 EPLD of Altera.The development enviroment is Max+PLUS__version8.3_.The results of the simulation is showed in Figure 5 and it tell us the scheme is workable.

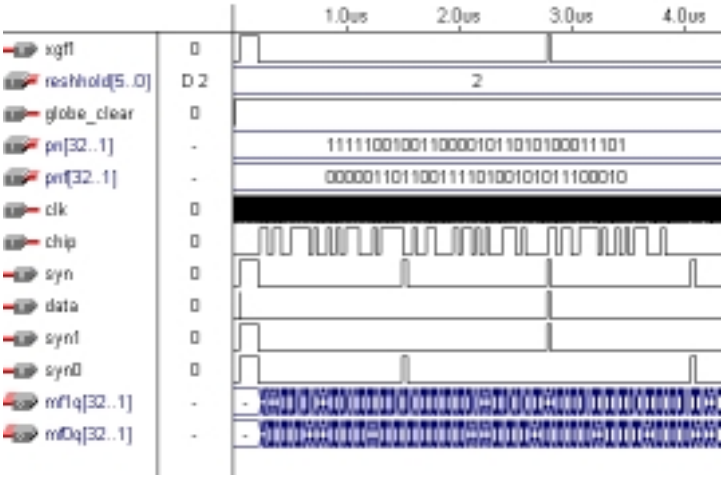

Figure 5 Simulation results

Conclution

We give a zero-IF digitized despreading scheme without PN code synchronization recovery in this paper. Through the theorial analysis is developed by some concrete data, generalization of the result is certain. The key factor is we want to give a analysis concept and method. The scheme passed the chip level simulaqtion, but still needs more examination in real radio channel.

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