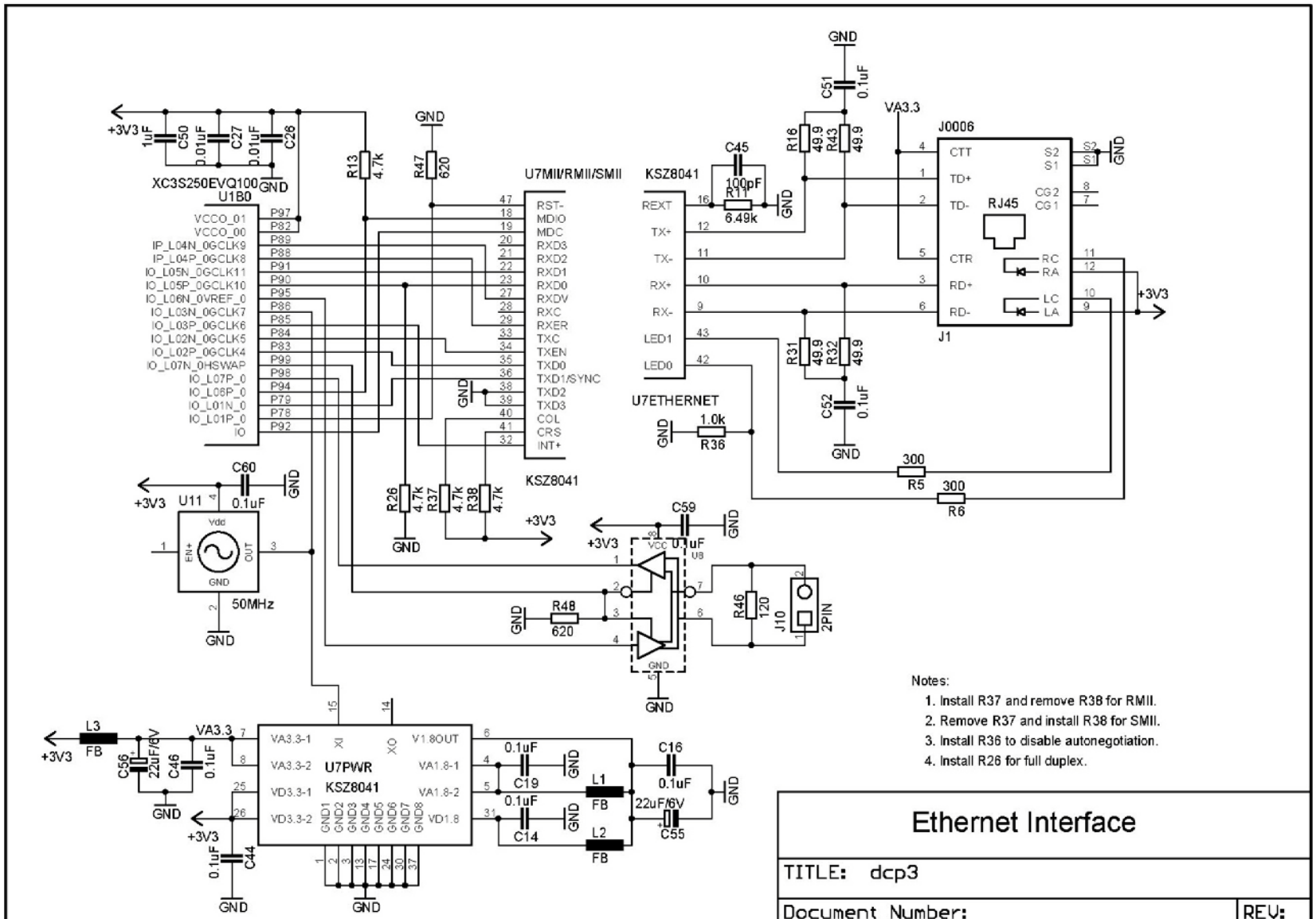
Appendix A – DCP-3 Schematic Diagram

The following 6 pages contain the schematic diagram of the DCP-3 digital signal processing PCB:

1. Ethernet Interface
2. High-speed Analog to Digital Converter
3. Serial Flash Memory and Low-speed DAC
4. High-speed Digital to Analog Converter
5. Voltage Regulator and JTAG Interface
6. Clock Oscillators

The schematic shows a Xilinx XC3S250E FPGA but the XC3S500E has the same pin configuration in the 100-pin TQFP package.



Ethernet Interface

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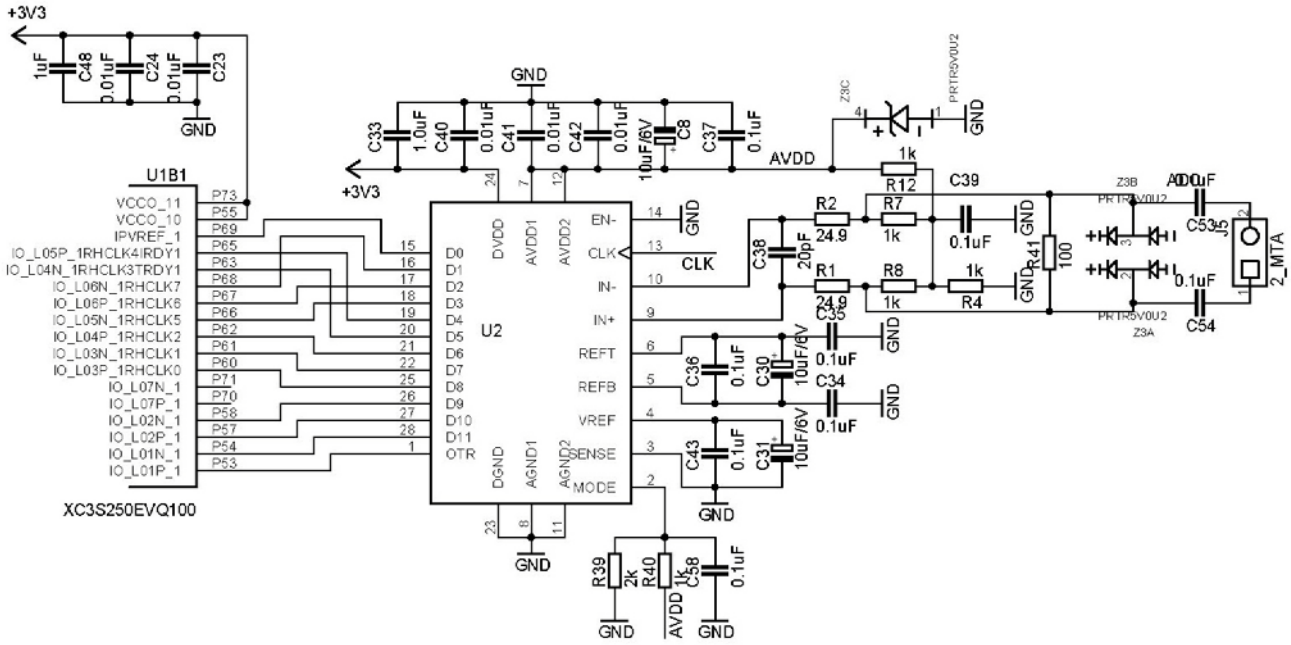

Notes:

1. Full-scale ADC input is 2.2 Vpp into 100 ohms (+8 dBm).
2. Minimum ADC input frequency is 1 MHz.
3. Mode pin is 2/3 Vcc to enable 2's complement output and duty cycle stabilizer.
4. Z3 is PRTR5V0U2X and is marked *R1.

80 Msps 12-bit ADC		
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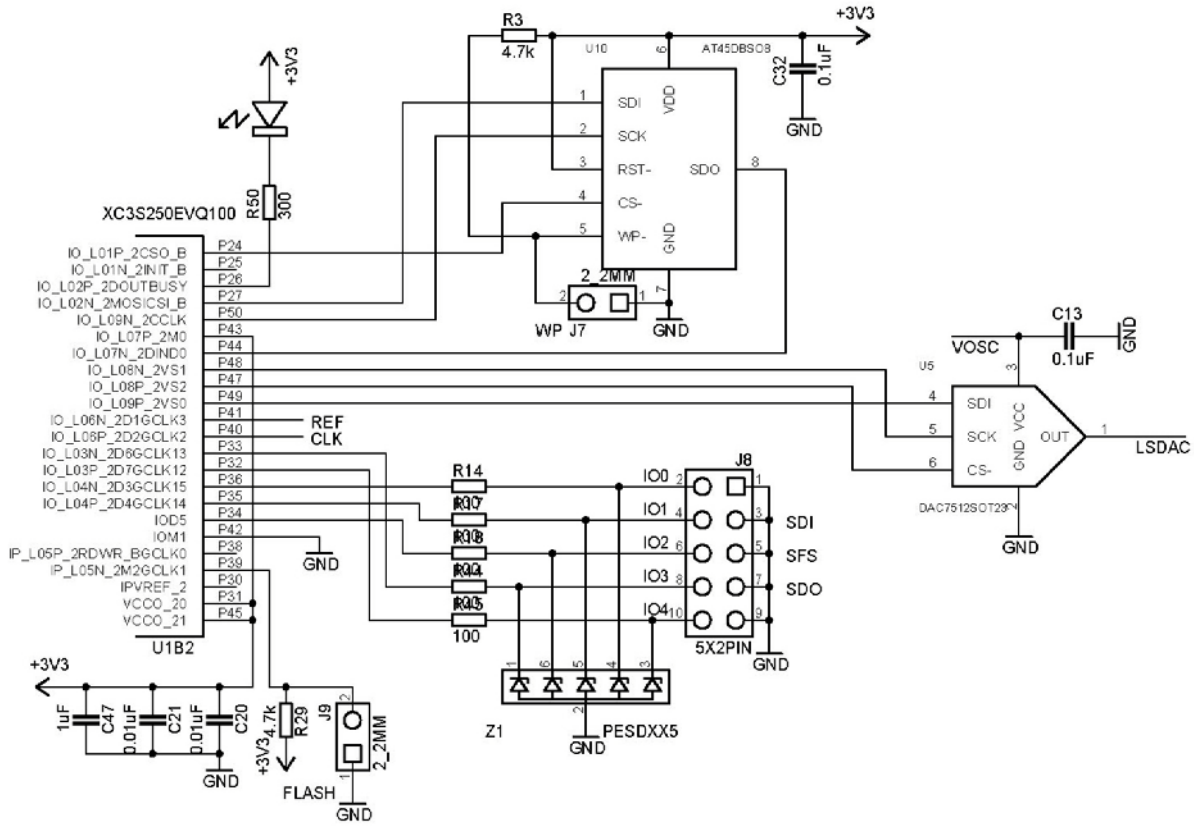

Notes:

1. Install shorting plug on J7 to boot from flash memory.
2. Remove shorting plug from J9 to program flash memory via JTAG port.
3. U5 and C13 may be removed when using external clock.
4. Z1 is PESD3V3L5UY and is marked K3*.

Serial Flash and Low Speed DAC	
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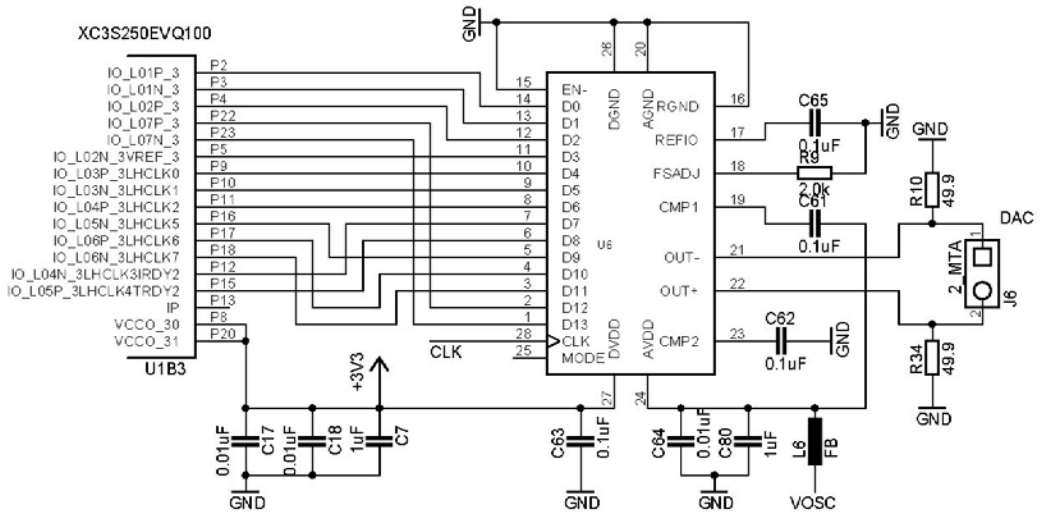

Notes:

1. DAC output is 1 Vpp into 100 ohms (+1 dBm).
2. Install L5 and remove L6 for 5V DAC.
3. Remove L5 and install L6 for 3.3V DAC.
4. Mode 0 selected - offset binary.

80 Msps 12-bit DAC		
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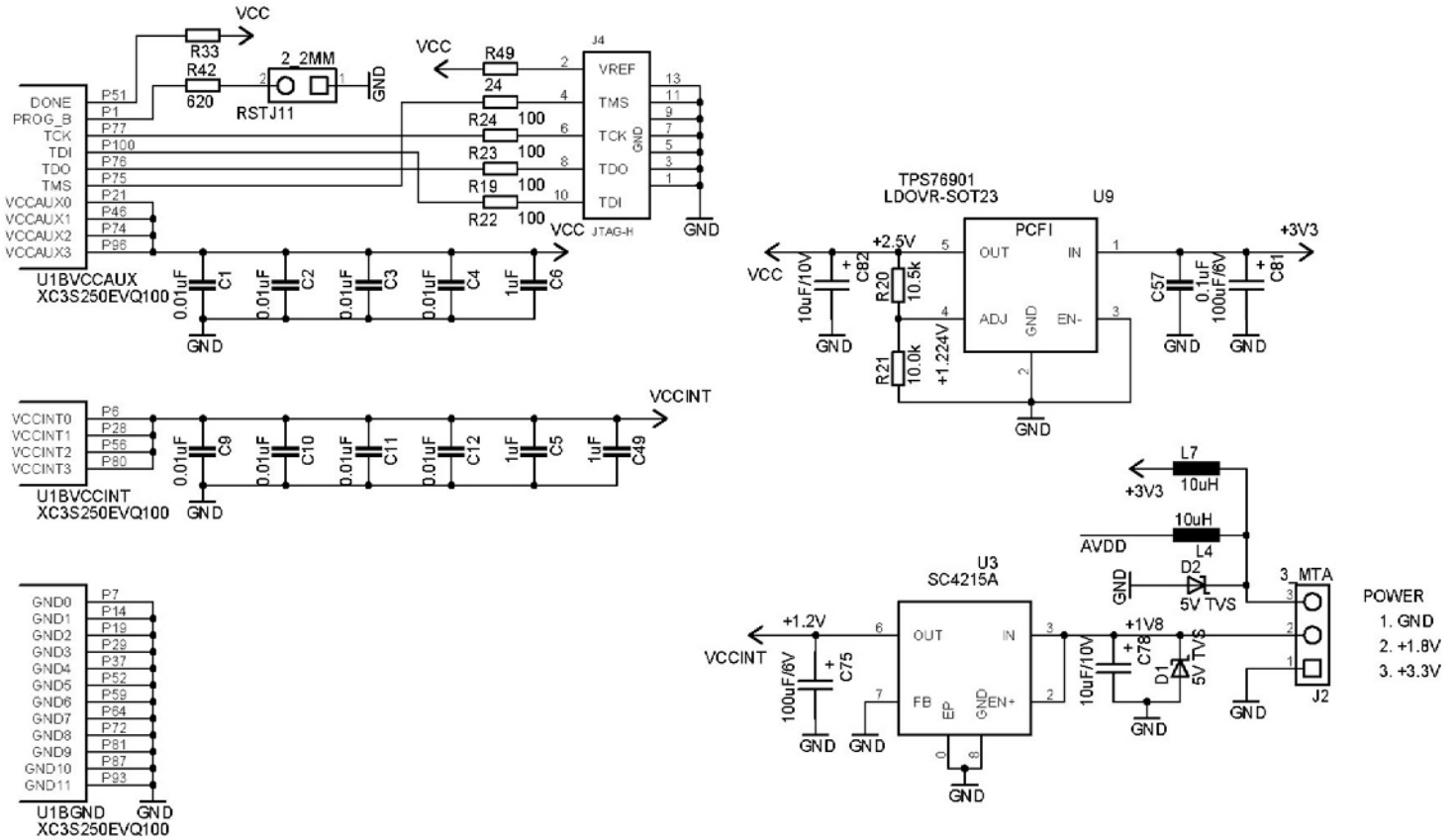

Notes:

1. Install J12 to reset FPGA and remove to initiate re-boot.
2. J4 supports Xilinx Platform USB cable for FPGA and flash memory programming.
3. Remove R20 and R21 when using TPS76925 at U9 (marked PCJI).

Voltage Regulators & JTAG Interface	
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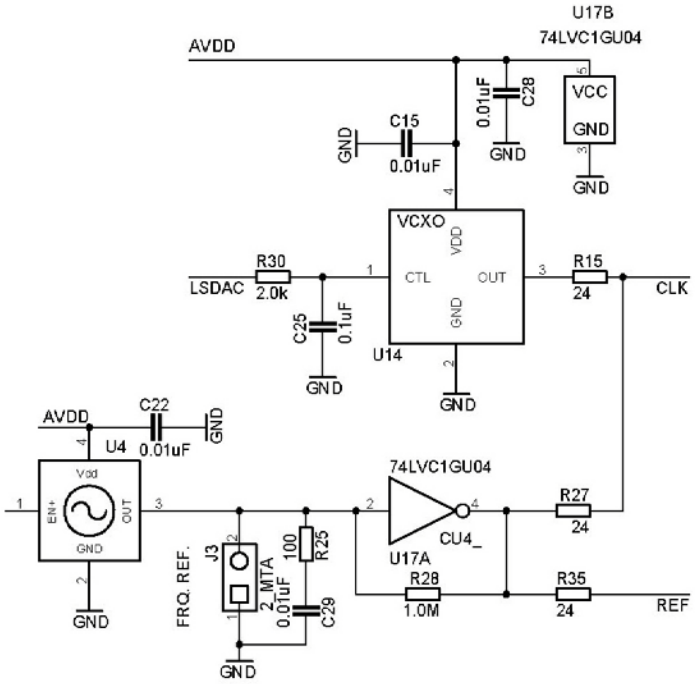

Notes:

1. Install R27 and remove R15 for external clock.
2. Install R35 for external frequency reference.
3. Install U14 for VCXO or U4 for fixed oscillator but not both.
4. R30, C15, C25, U4 and U14 may be removed when using external clock.

80 MHz VCXO (internal clock)	
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