The I²C bus standard was introduced in the mid-1980s to operate at a bit rate of up to 100 kbit/s, a rate that at that time required no special IC processes. In 1995 the standard was augmented with the addition of a *fast mode*, which allows up to 400 kbit/s transfers between devices that support it. Even at this faster rate, the updating of the output of one channel of the digital-to-analog converter takes over 500 μs with OSC = 4 MHz and over 100 μs with OSC = 20 MHz, more than an order of magnitude slower than a transfer takes using the serial peripheral interface discussed in Chapter 7 and more than two orders of magnitude slower than the update of one of the PIC's output ports.

In spite of its relatively slow speed, the I²C bus interface is widely used for many applications where its speed is still much faster than an application requires (e.g., reading the temperature from a transducer having a thermal time constant measured in seconds). Furthermore, once the bit-banging subroutines have been written, accessing an *additional* I²C device simply requires attaching it to the same two I²C lines going to all other I²C peripheral chips and then calling the same bit-banging subroutines used with the other chips.

This chapter begins with a discussion of the features of the I²C bus standard needed to deal with peripheral chips. Bit-banging subroutines will then be developed. Finally, these will be used in conjunction with the three chips mentioned earlier.

9.2 I²C BUS OPERATION

The I²C bus specification, "The I²C-Bus and how to use it," is available on the Internet and can be downloaded from **http://www.service.com/ps/philips53.html.** It requires two open-drain I/O pins. These two pins, called *SCL* (serial clock) and *SDA* (serial data), are implemented on the PIC chips as the two multipurpose pins

RC3/SCK/SCL

and

RC4/SDI/SDA

respectively.

The open-drain outputs for the SCL and SDA pins are achieved in a way that could use *any* of the PIC's I/O pins, as shown in Figure 9-1. To change the output from 0 V (Figure 9-1a) to a high-impedance output, instead of writing a one to the **PORTC** bit, a one is written to the corresponding **TRISC** bit, thereby obtaining the high impedance by turning the pin into a high-impedance input pin.

Whereas any of the PIC's I/O pins *could* be used to implement the SCL and SDA pins, there are two good reasons to use the RC3/SCK/SCL and RC4/SDI/SDA pins:

- The I²C circuitry controls the *slope* of the output changes on these pins to meet the I²C bus specifications.
- If an application utilizes this PIC as a slave to another PIC, these are the same two pins that the I²C slave mode uses *automatically*.

The I²C bus protocol includes a variety of features that are not needed for peripheral chip access (e.g., multimaster control). These unneeded features will be bypassed in this chapter.

Transfers on the I²C bus take place 9 bits at a time, as shown in Figure 9-2. The clock line, SCL, is driven by the PIC chip, which serves as bus master. The open-drain feature of every chip's bus driver can be used by the receiver to hold the clock line low, thereby signaling the transmitter to pause until